for Geoffrey

Access DB# 118981

SEARCH REQUEST FORM

Scientific and Technical Information Center

Requester's Full Name: James Seal Examiner #: 74900 Date: 05 April 2004
Art Unit: 2135 Phone Number 30 8-4562 Serial Number: 09748839
Mail Box and Bldg/Room Location: _____ Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

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Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

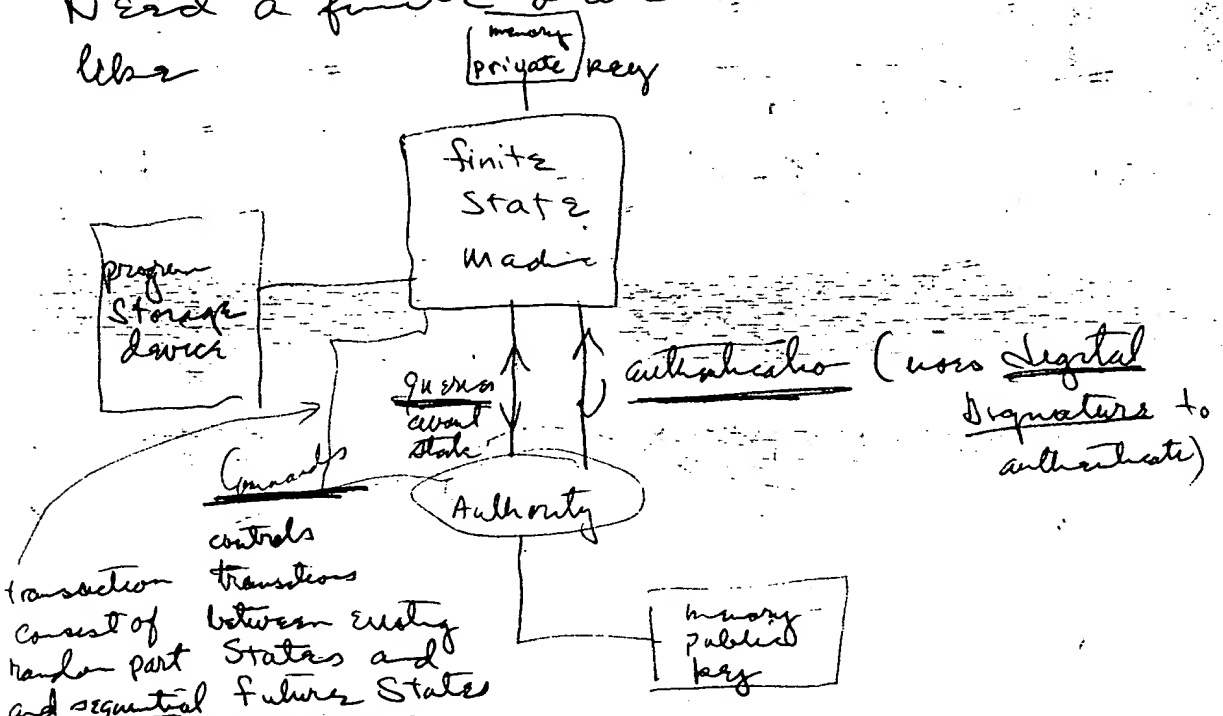
Title of Invention: Method and apparatus for providing public key Control for a cryptographic processor

Inventors (please provide full names): Ronald Smith, Edward P'Aveyron Robert Debellis, Randall Easter, Lucas Green

Earliest Priority Filing Date: 6/30/1997

**For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

Need a finite state machine that looks like =



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STAFF USE ONLY		Type of Search		Vendors and cost where applicable	
Searcher:	Geoffrey St. Leger	NA Sequence (#)		STN	
Searcher Phone #:	308-7800	AA Sequence (#)		Dialog	✓
Searcher Location:	4B30	Structure (#)		Questel/Orbit	
Date Searcher Picked Up:	4/7/4	Bibliographic	✓	Dr.Link	
Date Completed:	4/7/4	Litigation		Lexis/Nexis	
Searcher Prep & Review Time:	60	Fulltext	✓	Sequence Systems	
Clerical Prep Time:		Patent Family		WWW/Internet	
Online Time:	300	Other		Other (specify)	

PTO-1590 (8-01)

File 347:JAPIO Nov 1976-2003/Dec(Updated 040402)
(c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200418
(c) 2004 Thomson Derwent

Set	Items	Description
S1	2915	(STATE OR STATEFUL)()(MACHINE? ? OR DIAGRAM? ?) OR FINITE(-)STATE? ?
S2	11515	(CURRENT OR RECENT OR EXISTING OR PRESENT)(1W)(STATE? ? OR CONDITION? ?)
S3	3101	(PAST OR PREVIOUS OR PRIOR OR PRECEDING OR LAST OR EARLIER OR FORMER)(1W)(STATE? ? OR CONDITION? ?)
S4	55328	(FUTURE OR ALLOWED OR ALLOWABLE OR PERMITTED OR PERMISSABLE OR AUTHORIZED OR AUTHORISED OR ACCEPTED OR ACCEPTABLE OR NORMAL OR EXPECTED OR RANGE? ?)(5N)(STATE? ? OR CONDITION? ?)
S5	1123	DIGITAL()SIGNATURE? ?
S6	[illegible]	(PUBLIC OR PRIVATE)()KEY? ?
S7	[illegible]	CRYPTO? OR CRYPTANALY? OR CIPHER? OR CYPHER? OR ENCRYPT? OR ENCIPHER? OR SCRAMBL? OR DECRYPT? OR DECIPHER? OR UNENCRYPT? OR UNSCRAMBL?
S8	2	S1 AND S2:S4 AND S5:S7
S9	51	S1 AND S5:S7
S10	51	S8:S9
S11	2514	(STATE OR STATEFUL)()MACHINE? ? OR FINITE()STATE? ?
S12	212	S11 AND S2:S4
S13	22	S11 AND S2 AND S3:S4
S14	3	S11 AND S3 AND S4
S15	23	S13:S14
S16	22	S15 NOT S10
S17	150	S11 AND S2
S18	32	S11 AND S3
S19	55	S11 AND S4
S20	212	S17:S19
S21	7741	S2:S4(10N)(MACHINE? ? OR DEVICE? ? OR UNIT OR UNITS OR HARDWARE OR AUTOMATION OR DESIGN? OR MANUFACTUR? OR ENGINEER?)
S22	105	S20 AND S21
S23	1113064	AUTHENTICAT? OR SECUR? OR SAFE??
S24	7	S20 AND S23
S25	620	FINITE()STATE? ?
S26	64	S20 AND S25
S27	26	S22 AND S26
S28	33	S24 OR S27
S29	28	S28 NOT (S10 OR S16)
S30	66	S11 AND S23
S31	47	S30 NOT (S10 OR S16 OR S29)
S32	12	S25 AND S31
S33	690405	CONTROLLER? ?
S34	35	S31 NOT S32
S35	8	S33 AND S34
S36	27	S34 NOT S35

16/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06927327 **Image available**
STATE MACHINE EQUIPPED WITH DEBUG FUNCTION AND SEMICONDUCTOR DEVICE

PUB. NO.: 2001-154868 [JP 2001154868 A]
PUBLISHED: June 08, 2001 (20010608)
INVENTOR(s): SATO HISAO
KUWAZAWA ATSUSHI
TSUJI RYUICHI
APPLICANT(s): SEIKO EPSON CORP
APPL. NO.: 11-338154 [JP 99338154]
FILED: November 29, 1999 (19991129)
INTL CLASS: G06F-011/22; G01R-031/3185; G01R-031/28

ABSTRACT
PROBLEM TO BE SOLVED: To provide a **state machine** having an excellent debug function for facilitating a countermeasure to specification change without changing hardware and a semiconductor device having the **state machine** .

SOLUTION: This **state machine** is provided with a **state machine** 30 for control having a normal operation mode realizing transition from a present **state** being a **present state** held in a **present state** register 26 to the next state being the next state and a debug mode realizing transition from the **state** of the **normal** operation mode to a debug **state** . This **state machine** is provided with a state detecting part 27 for detecting the **state** of the **normal** operation mode matched with a designated state being the detection condition. In this case, when the **state** of the **normal** operation module matched with the designated state is detected by the state detecting part 27, the transition of the **state machine** 30 for control from the **state** of the **normal** operation mode to the debug **state** is realized so that the transition of the **state machine** 30 for control in the normal operation mode can be stopped.

16/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06839722 **Image available**
CONTROL UNIT AND MANUFACTURE OF THE SAME

PUB. NO.: 2001-067217 [JP 2001067217 A]
PUBLISHED: March 16, 2001 (20010316)
INVENTOR(s): ARCIDIACONO LILIANA
MATRANGA VINCENZO
APPLICANT(s): STMICROELECTRONICS SRL
APPL. NO.: 2000-180278 [JP 2000180278]
FILED: June 15, 2000 (20000615)
PRIORITY: 99830375 [EP 99830375], EP (European Patent Office), June 16, 1999 (19990616)
INTL CLASS: G06F-009/22

ABSTRACT
PROBLEM TO BE SOLVED: To provide a control unit in which the design stage of unit is simplified to the maximum level.

SOLUTION: This is a control unit for electronic microcontroller or microprocessor and a method for manufacturing the control unit. In this control unit, a **finite state machine** is manufactured from plural control sub-units 2, and each sub-unit 2 is made correspond to one logic combination network, and each unit in plural control sub-units 2 is independently connected with an arbitrating block 3 so that information

related with a **state** available in the **future** can be offered, and a **present** **state** command can be received.

16/5/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014587303 **Image available**
WPI Acc No: 2002-408007/200244
Related WPI Acc No: 2002-408006
XRPX Acc No: N02-320518
Method and device for decoding symbol strings for application relates to telecommunications networks, base and mobile communications stations, with reduced hardware requirement
Patent Assignee: CANON KK (CANO); LE BARS P (LBAR-I); OLIER S (OLIE-I)
Inventor: LE BARS P; OLIER S
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2814300	A1	20020322	FR 200011899	A	20000918	200244	B
US 20020065859	A1	20020530	US 2001953254	A	20010917	200244	

Priority Applications (No Type Date): FR 200011899 A 20000918; FR 200011898 A 20000918
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2814300	A1		46	H03M-013/27	
US 20020065859	A1			G06F-001/00	

Abstract (Basic): FR 2814300 A1
NOVELTY - For symbols connected by a predetermined parity relationship, previously created by a coder, their estimation is realized with a function having several components for calculating probabilities associated with the state of the coder. The probabilities are of three types (alphak, betak, Lke), the first resulting from the effect of **previous** **states** on the **current** **state** , the second from the **current** **state** and the third according to whether a symbol belongs to a coding alphabet.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is made for a device for decoding symbol strings with a specific multiplexor (12) controlled by a **state** **machine** (14) with a computer (10) such that the three types of probability can be determined using the same circuit.
USE - Decoding symbol strings. The invention relates to telecommunications networks, base and mobile communications stations.
ADVANTAGE - A single circuit can be used for determining all past, **present** and **state** probabilities.
DESCRIPTION OF DRAWING(S) - (Drawing includes non-English language text). Figure shows a block diagram of the invention.
probabilities (alphak, betak, Lke)
multiplexor (12)
state **machine** (12)
computer. (10)
pp; 46 DwgNo 6/16
Title Terms: METHOD; DEVICE; DECODE; SYMBOL; STRING; APPLY; RELATED; TELECOMMUNICATION; NETWORK; BASE; MOBILE; COMMUNICATE; STATION; REDUCE; HARDWARE; REQUIRE
Derwent Class: T01; U21; W01; W02
International Patent Class (Main): G06F-001/00; H03M-013/27
International Patent Class (Additional): G06F-017/00; H04L-012/56; H03M-007/24
File Segment: EPI

16/5/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

14163607 **Image available**
WPI Acc No: 2001-637826/200173
Related WPI Acc No: 2000-474595
XRPX Acc No: N01-476657

Approximate weighted finite - state automaton generating method in automatic speech recognition, involves creating transition of automaton from current to previous state if proposed new state is similar to previous state

Patent Assignee: AT & T CORP (AMTT)
Inventor: BUCHSBAUM A L; GIANCARLO R; WESTBROOK J R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6266634	B1	20010724	US 97975648	A	19971121	200173	B
			US 2000533549	A	20000323		

Priority Applications (No Type Date): US 97975648 A 19971121; US 2000533549 A 20000323
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6266634	B1		25	G10L-015/14	Cont of application US 97975648 Cont of patent US 6073098

Abstract (Basic): US 6266634 B1

NOVELTY - Non-deterministic weighted **finite - state** automaton is determinized to form approximate weighted **finite - state** automaton on a state-by-state basis. If proposed new state of approximate weighted **finite - state** automaton is sufficiently similar to **previous state**, a transition from **current state** to **previous state** is created. Otherwise transition from **current state** to proposed new state is created.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for approximate weighted **finite - state** automaton generating system.

USE - For generating an approximate weighted **finite - state** automaton used in automatic speech recognition.

ADVANTAGE - Generates deterministic weighted **finite - state** automaton having improved size reductions. The approximate weighted **finite - state** automata require less memory. The approximation used to generate the approximate weighted **finite - state** automata do not degrade the accuracy or precision of the automatic speech recognition process.

DESCRIPTION OF DRAWING(S) - The figure shows the outline of automatic speech recognition process.

pp; 25 DwgNo 2A/18

Title Terms: APPROXIMATE; WEIGHT; FINITE; STATE; AUTOMATIC; GENERATE; METHOD; AUTOMATIC; SPEECH; RECOGNISE; TRANSITION; AUTOMATIC; CURRENT; STATE; PROPOSED; NEW; STATE; SIMILAR; STATE
Derwent Class: P86; T01; W04
International Patent Class (Main): G10L-015/14
International Patent Class (Additional): G06M-009/00
File Segment: EPI; EngPI

16/5/5 **(Item 3 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
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014096600 **Image available**
WPI Acc No: 2001-580814/200165
XRPX Acc No: N01-432588

State transition method in interactive computer-based training e.g. for Internet, has interdependent, state - machine -based hardware and software simulators for emulating hardware and software functionality

Patent Assignee: MCI WORLDCOM INC (MCIW-N)
Inventor: CLOSSEN J R; DOGGETT P J; WALL R S; WARNER D R
Number of Countries: 094 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200135187	A2	20010517	WO 2000US30879	A	20001109	200165	B
AU 200115941	A	20010606	AU 200115941	A	20001109	200165	
EP 1292868	A2	20030319	EP 2000978482	A	20001109	200322	
			WO 2000US30879	A	20001109		
BR 200015455	A	20030722	BR 200015455	A	20001109	200365	
			WO 2000US30879	A	20001109		

Priority Applications (No Type Date): US 99436553 A 19991109

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200135187	A2	E	43	G06F-000/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

[illegible]	A	G06F-000/00	Based on patent WO 200135187
[illegible]	A2 E	G06F-001/00	Based on patent WO 200135187

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR

BR 200015455	A	G06G-007/48	Based on patent WO 200135187

Abstract (Basic): WO 200135187 A2

NOVELTY - State transition method effectuated in a computer-readable memory system includes the steps of: identifying a **current state** of the **state machine** where a transition is to be effectuated; determining if there is a state immediately prior to the **current state** , and if so, determining whether there is a dependency of the **current state** on the immediately **prior state** , the dependency being characterized as a first order dependency; inferring a reference value associated with the **current state** based on the first order dependency; and determining a **future** state of the **state machine** based on the inferred reference value.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) state transition inference engine;

(b) **state machine** for simulating hardware functionality

USE - For Internet, Intranet, etc.

ADVANTAGE - Training is flexible and can be accessed from anywhere and at any time using the Internet. Classes can be tailored to every individual's proficiency level.

DESCRIPTION OF DRAWING(S) - The block diagram shows an on-line interactive CBT system

CBT web-based training (206)

Server (204)

Client (208)

pp; 43 DwgNo 2/11

Title Terms: STATE; TRANSITION; METHOD; INTERACT; COMPUTER; BASED; TRAINING ; INTERDEPENDENT; STATE; MACHINE; BASED; HARDWARE; SOFTWARE; SIMULATE; EMULATION; HARDWARE; SOFTWARE; FUNCTION

Derwent Class: T01

International Patent Class (Main): G06F-000/00; G06F-001/00; G06G-007/48

International Patent Class (Additional): G06F-009/45; G06F-009/455; G06F-017/50; G06G-007/62

File Segment: EPI

16/5/6 **(Item 4 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

014095659 **Image available**

WPI Acc No: 2001-579873/200165

XRPX Acc No: N01-431685

Microprocessor for e.g. portable computer, portable communication device,

has logic circuits which individually evaluate predetermined instructions received by microcode units providing control signals

Patent Assignee: MOORE W P (MOOR-I); VENTRONE S T (VENT-I)
Inventor: MOORE W P; VENTRONE S T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010010082	A1	20010726	US 98128503	A	19980803	200165	B
			US 2001805200	A	20010314		

Priority Applications (No Type Date): US 98128503 A 19980803; US 2001805200 A 20010314
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010010082	A1		15	G06F-001/26	Div ex application US 98128503 Div ex patent US 6237101

Abstract (Basic): US 20010010082 A1

NOVELTY - Each microcode unit (32) outputs a control signal for instruction execution. The input units respectively receive an instruction address and a control variable corresponding to a microprocessor **current state** . A control signal input unit receives the control signals from the microcode unit for preceding instruction. Logic circuits evaluate the instruction received by microcode unit.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) a microprocessor system;
(b) microprocessor power reduction method;
(c) a **state machine** control logic production method;
(d) a **state machine** decoding method;
(e) and a signal-bearing medium.

USE - For e.g. portable computer, portable communication device e.g. portable telephone, cellular phone, pager, portable device e.g. smart card

ADVANTAGE - Attains reduction of power consumption since control signal of next cycle can be derived based on function of next cycle along with **previous** cycle **state** , thereby lengthening service life of battery for portable computer and computer applications. Enables reducing toggle of microprocessor by controlling control signals, thus reducing thermal dissipation, heat shrinking and battery power consumption.

DESCRIPTION OF DRAWING(S) - The figure shows the structure of microprocessor.

Microcode unit (32)

pp; 15 DwgNo 3A/5

Title Terms: MICROPROCESSOR; PORTABLE; COMPUTER; PORTABLE; COMMUNICATE; DEVICE; LOGIC; CIRCUIT; INDIVIDUAL; EVALUATE; PREDETERMINED; INSTRUCTION; RECEIVE; UNIT; CONTROL; SIGNAL
Derwent Class: T01
International Patent Class (Main): G06F-001/26
International Patent Class (Additional): G06F-001/28; G06F-001/30
File Segment: EPI

16/5/7 **(Item 5 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

Patent No: 2001-301834/200132
WPIX Acc No: N01-216695

Control unit for electronic microcontrollers and microprocessors consists of a number of sub-units each corresponding to one combinational logic network and each independently connected to an arbitrator to receive state commands

Patent Assignee: STMICROELECTRONICS SRL (SGSA)
Inventor: ARCIDIACONO L; MATRANGA V
Number of Countries: 027 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1061437	A1	20001220	EP 99830375	A	19990616	200132	B
JP 2001067217	A	20010316	JP 2000180278	A	20000615	200132	
US 6668199	B1	20031223	US 2000595759	A	20000616	200408	

Priority Applications (No Type Date): EP 99830375 A 19990616
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1061437	A1	E	16	G06F-009/318	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

JP 2001067217	A		12	G06F-009/22
US 6668199	B1			G05B-011/01

Abstract (Basic): EP 1061437 A1

NOVELTY - The control unit forms a **finite state machine** consisting of combinational logic circuits and includes a number of separate sub-units each corresponding t one combinational logic circuit. Each sub-unit is connected to an arbitration block to provide information about a possible **future state** and receive a **present state** command. The sub-units can each be defined in terms of Very High Speed Integrated Circuit Hardware Description Language.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a method of making a control unit for electronic microcontrollers and microprocessors.

USE - In electronic microcontroller and microprocessor control units.

ADVANTAGE - Splitting the unit into sub-units simplifies the manufacture and programming as each sub-unit can be dealt with independently of the rest.

pp; 16 DwgNo 0/8

Title Terms: CONTROL; UNIT; ELECTRONIC; MICROPROCESSOR; CONSIST; NUMBER; SUB; UNIT; CORRESPOND; ONE; COMBINATION; LOGIC; NETWORK; INDEPENDENT; CONNECT; ARBITER; RECEIVE; STATE; COMMAND
Derwent Class: T01; T06; U21
International Patent Class (Main): G05B-011/01; G06F-009/22; G06F-009/318
File Segment: EPI

16/5/8 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013455737 **Image available**
WPI Acc No: 2000-627680/200060
Related WPI Acc No: 1999-070024
XRPX Acc No: N00-465025

Interruptible state machine for use in bi-directional movement of error free data, has stack register to receive state from decoder in absence of interrupt or to receive interrupt vectors in presence of interrupt

Patent Assignee: CYPRESS SEMICONDUCTOR CORP (CYPR-N)
Inventor: GRIVNA E L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6081866	A	20000627	US 96780167	A	19961226	200060	B
			US 98200373	A	19981124		

Priority Applications (No Type Date): US 96780167 A 19961226; US 98200373 A 19981124
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6081866	A		16	G06F-009/46	Cont of application US 96780167 Cont of patent US 5850556

Abstract (Basic): US 6081866 A

NOVELTY - An interruptible **state machine** (200) has next state

decoder (202) to **present** a **state** . An interrupt processor has interrupt vectors (212) and storage register (208) to store the state. A stack register (204) in communication with decoder and interrupt processor receives the state from decoder in the absence of an interrupt or receives interrupt vectors in the presence of interrupt.

DETAILED DESCRIPTION - The decoder is connected to multiplexer (210). The storage register is connected in parallel between decoder and multiplexer. Interrupt vector is connected to multiplexer which is connected to stack register. INDEPENDENT CLAIMS are also included for the following:

(a) method to prevent state from loading into a stack register;

(b) method to service an interrupt

USE - For use in digital communication for bi-directional movement of error free digital data in computer interfaces such as parallel ports, serial ports, modems, bus and network interfaces.

ADVANTAGE - The **state machine** simplifies the implementation of a controller for data movers. The machine is adapted to have any number of **normal states** for more than one input or interrupt. It solves the complexity problem in the **state machine** environment such as pipelined data paths of RISC processors and data flow architecture **state machines** . The **state machines** are also implemented as computer program instructions.

DESCRIPTION OF DRAWING(S) - The figure shows block diagram of interruptible **state machine** .

Interruptible **state machine** (200)

Next state decoder (202)

Stack registers (204)

Storage register (208)

Multiplexer (210)

Interrupt vectors (212)

pp; 16 DwgNo 13/14

Title Terms: STATE; MACHINE; BI; DIRECTION; MOVEMENT; ERROR; FREE; DATA; STACK; REGISTER; RECEIVE; STATE; DECODE; ABSENCE; INTERRUPT; RECEIVE; INTERRUPT; VECTOR; PRESENCE; INTERRUPT

Derwent Class: T01

International Patent Class (Main): G06F-009/46

File Segment: EPI

16/5/9 **(Item 7 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

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image available

WPI Acc No: 2000-474595/200041

Related WPI Acc No: 2001-637826

XRPX Acc No: N00-354006

Automatic speech recognition method, involves determining non-deterministic weighted finite state lattice of proposed new state is similar to previous state of lattice

Patent Assignee: AT & T CORP (AMTT)

Inventor: BUCHSBAUM A L; GIANCARLO R; WESTBROOK J R

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6073098	A	20000606	US 97975648	A	19971121	200041	B

Priority Applications (No Type Date): US 97975648 A 19971121

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6073098	A		24	G10L-015/08	

Abstract (Basic): US 6073098 A

NOVELTY - The input electrical signal representing uttered speech is converted to vector lattice and then to recognized text string using approximate weighted **finite state** lattice. The set of states of non-deterministic weighted **finite state** lattice is determined from **current state** of approximate weighted **finite state** lattice if

proposed new state is similar to **previous state** of lattice.

DETAILED DESCRIPTION - The transition from the **current state** of approximate weighted **finite state** lattice to the proposed state lattice to **previous state** of proposed new state is not similar to **previous state** . An INDEPENDENT CLAIM is also included for automatic speech recognizing systems.

USE - For generating approximate weighted **finite state** automata.

ADVANTAGE - Size reduction is achieved. Since composition is associative, it can be computed in most efficient manner.

DESCRIPTION OF DRAWING(S) - The figure shows graph plotting the number of weighted **finite state** automata.

pp; 24 DwgNo 7/18

Title Terms: AUTOMATIC; SPEECH; RECOGNISE; METHOD; DETERMINE; NON; WEIGHT; FINITE; STATE; LATTICE; PROPOSED; NEW; STATE; SIMILAR; STATE; LATTICE
Derwent Class: P86; W04
International Patent Class (Main): G10L-015/08
File Segment: EPI; EngPI

16/5/10 **(Item 8 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
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image available
1999-471377/199940
N99-352164

High frequency functioning state machine

Patent Assignee: SGS THOMSON MICROELTRN SA (SGSA)
Inventor: RAMANADIN B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2775142	A1	19990820	FR 982161	A	19980219	199940	B

Priority Applications (No Type Date): FR 982161 A 19980219
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2775142	A1		17	H03K-005/13	

Abstract (Basic): FR 2775142 A1

NOVELTY - There is a second register and combination logic circuit, allowing future commands to be memorised during an active clock cycle period. A slave circuit is not needed.

USE - Integrated circuits with **state machines** .

ADVANTAGE - The **state machine** architecture allows circuit combinations to be obtained with reduced propagation time and not dependent on the commanded circuit propagation time.

DESCRIPTION OF DRAWING(S) - The figure shows the **state machine**

state machine (5)
first register (R1)
second register (R2)
current state (EC)
clock signal (HCK)
first combined logic circuit (C1)
second combined logic circuit (C2)
input (I)
future state (EF)

pp; 17 DwgNo 3/5

Title Terms: HIGH; FREQUENCY; FUNCTION; STATE; MACHINE
Derwent Class: U22
International Patent Class (Main): H03K-005/13
International Patent Class (Additional): H03K-005/15
File Segment: EPI

16/5/11 **(Item 9 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

C12550305 **Image available**
WPI Acc No: 1999-356411/199930
XRPX Acc No: N99-265245
Software programmable state machine **for use within integrated circuit of computer**
Patent Assignee: INTEL CORP (ITLC)
Inventor: O'CONNOR D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5905902	A	19990518	US 95537155	A	19950928	199930	B

Priority Applications (No Type Date): US 95537155 A 19950928
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
	A		14	G06F-013/00	

(Basic): US 5905902 A
NOVELTY - A comparator (204) compares **current state** and current input values with the masked values stored in a tag array (209). If there is a match, the next state array (211) is controlled to output next state corresponding to the **current** input **state** .
DETAILED DESCRIPTION - A tag array (209) selectively stores a subset of N2 possible transitions corresponding to permissible transitions. Each permissible transition has a combination of a **current state** and a current input value. A next state array (211) stores next state associated with each combination of **current states** and current input values. A mask value is provided for each **current state** and current values stored in the tag array.
USE - For computer system, traffic lights and elevators.
ADVANTAGE - Requires minimal memory since a cache like arrangement is used and stores only **allowable** or permissible transitions and new **states** corresponding to those transitions. Thus the cost of the **state machine** is reduced.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the programmable **state machine** .
Comparator (204)
Tag array (209)
State array (211)
pp; 14 DwgNo 7/9
Title Terms: SOFTWARE; PROGRAM; STATE; MACHINE; INTEGRATE; CIRCUIT; COMPUTER
Derwent Class: T01
International Patent Class (Main): G06F-013/00
File Segment: EPI

16/5/12 **(Item 10 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

012050182 **Image available**
WPI Acc No: 1998-467092/199840
XRPX Acc No: N98-363923
Patch mechanism for dynamic modification of behaviour of state machine **- has logic unit coupled to** state machine **and multiplexer, which outputs signal to multiplexer when modification of individual state is valid**
Patent Assignee: VLSI TECHNOLOGY INC (VLSI-N)
Inventor: CHAMBERS P; SHELTON R L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5796994	A	19980818	US 97792713	A	19970130	199840	B

Priority Applications (No Type Date): US 97792713 A 19970130

Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
US 5796994   A   9 G06F-001/04

Abstract (Basic): US 5796994 A
The mechanism (50) includes a PLA (52) for storing a modified transition for an individual state of a **state machine** (20) to be modified from a **current state** to a modified successive state. The PLA also stores a modified output transition for the individual state to be modified from a **current** output **state** to a modified successive output state.
A pair of multiplexers (54,56) is provided, whose input terminals are coupled to the **state machine** and the PLA for allowing the modifier to select an unmodified current transition defined by the machine and the modifier. The **state machine** is also **allowed** to select an unmodified output transition defined by the **state machine** and the modified output transition by the multiplexer. A logic unit (38) is coupled to the **state machine** and multiplexer for signalling the multiplexer, when it is valid to modify the individual state from the unmodified current transition to the modified transition and from the unmodified output transition to the modified output transition.
USE - For silicon design.
ADVANTAGE - Produces dynamically modifiable synchronous **state machine** implementable using minimum amount of silicon area. Suppresses influence on performance and **normal** operation of **state machine** . Enables arbitrary modification of behaviour of **state machine** .
Dwg.2/2
Title Terms: PATCH; MECHANISM; DYNAMIC; MODIFIED; BEHAVE; STATE; MACHINE; LOGIC; UNIT; COUPLE; STATE; MACHINE; MULTIPLEX; OUTPUT; SIGNAL; MULTIPLEX ; MODIFIED; INDIVIDUAL; STATE; VALID
Derwent Class: T01
International Patent Class (Main): G06F-001/04
File Segment: EPI

16/5/13 **(Item 11 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
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Image available
WPI Acc No: 1995-392130/199550
XRPX Acc No: N95-285870
State machine **digital signal synchroniser for telecommunications applications - receives frame-based signal and stores in SRAM bit-defined states of predefined bit locations in frame and uses lookup table to change states based on** previous state **and incoming bit of signal**
Patent Assignee: SIEMENS TELECOM SYSTEM LTD (SIEI); TRANSWITCH CORP (TRAN-N); SIEMENS TELECOM SYSTEMS LTD (SIEI)
Inventor: JANG S; PARRELLA E L; CHANG S
Number of Countries: 002 Number of Patents: 002
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
TW 258849 A 19951001 TW 94108615 A 19940917 199550 B
US 5615237 A 19970325 US 94308083 A 19940916 199718

Priority Applications (No Type Date): US 94308083 A 19940916
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
TW 258849   A   8 H04L-007/00
US 5615237   A   17 H04L-007/00

Abstract (Basic): TW 258849 A
The synchroniser has an interface to receive bits of a telecommunications signal in a frame. A SRAM memory stores bit-defined states for a number of bit locations in the frame. A state update lookup table changes the states for a number of the frame bit locations in the SRAM based on a **previous state** and on an incoming bit of the signal.

Frame location identification logic determines the location of the signal frame's overhead bit based on the states of the bit locations. Pref. the SRAM is an x by y bit SRAM, where x equals the number of bits in the frame, and y is large enough so that the number of possible states <= 2y. Alternatively, bit locations may be divided into subgroups or stages and bits are used for state updates after the state of a previous stage reaches a predetermined threshold.

Dwg.1/10

Title Terms: STATE; MACHINE; DIGITAL; SIGNAL; SYNCHRONISATION; TELECOMMUNICATION; APPLY; RECEIVE; FRAME; BASED; SIGNAL; STORAGE; SRAM; BIT; DEFINE; STATE; PREDEFINED; BIT; LOCATE; FRAME; TABLE; CHANGE; STATE; BASED; STATE; INCOMING; BIT; SIGNAL

Derwent Class: W01

International Patent Class (Main): H04L-007/00

International Patent Class (Additional): H04J-003/06

File Segment: EPI

16/5/14 (Item 12 from file: 350)

Image available

WPI Acc No: 1995-240307/199531

Related WPI Acc No: 1999-070054; 1999-403770; 1999-404055; 1999-404056; 1999-456293; 1999-600343; 2000-052130; 2000-586103; 2000-636971; 2000-637172

XRPX Acc No: N95-187431

Speech recognition system user instruction method - allowing user to receive corresponding succession of instruction messages and exercises, selected in response to scoring of user

Patent Assignee: DRAGON SYSTEMS INC (DRAG-N)

Inventor: BAKER J K; GOULD J M; STEELE E E

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5428707	A	19950627	US 92976413	A	19921113	199531	B

Priority Applications (No Type Date): US 92976413 A 19921113

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5428707	A		85	G10L-009/00	

Abstract (Basic): US 5428707 A

The method involves definition of a **state machine** having a number of states and a set of one or more **allowed** response words for each such **state** and associating with each such response word a new state which the **state machine** will enter in response to the detection of a user generated signal as that response word, with the number of allowed response words associated with each such state being less than N. When the **state machine** is in each of a first set of the states, a user is sent one or more instruction messages associated with that state to teach the user how to use the recognition system. When the **state machine** is in states of a second set of the states, the user is presented with recognition exercises which simulate use of the recognition system for the task which uses a vocabulary of N or more words, but which prompts the user to produce a user generated signal representing a word corresponding to one of the smaller number of response words **allowed** for the **current state** of the second set. When the **state machine** is in each of the states, an automatic signal matching device is used to score closeness of matches between a user generated signal and models for each of a number of words, including at least the response words **allowed** for that **state** .

The method then responds to the scores produced by the matching device to select which of the response words **allowed** for the **current state** probably corresponds to the user generated signal for that state and advancing the **state machine** to the state associated with that selected response word. The user can progress through a succession of the states, to receive a corresponding succession of instruction

messages and exercises, selected in response to the scoring of his or her user generate signals against allowed response words.

ADVANTAGE - Increased ease and accuracy with which user can train system to understand his words.

Dwg.4/59

Title Terms: SPEECH; RECOGNISE; SYSTEM; USER; INSTRUCTION; METHOD; ALLOW; USER; RECEIVE; CORRESPOND; SUCCESSION; INSTRUCTION; MESSAGE; EXERCISE; SELECT; RESPOND; SCORE; USER

Derwent Class: P86; W04

International Patent Class (Main): G10L-009/00

File Segment: EPI; EngPI

16/5/15 **(Item 13 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

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009022352 **Image available**

WPI Acc No: 1992-149726/199218

XRPX Acc No: N92-111909

State machine **for controlling cardiac stimulator - selects different rates of adjustment so gain level for sense amplifiers can be adjusted without significant overshoot**

Patent Assignee: INTERMEDICS INC (INTE-N)

Inventor: BAKER R G; VANDEGRIFF J W; WOODSON D L

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5103819	A	19920414	US 90540852	A	19900620	199218	B

Priority Applications (No Type Date): US 90540852 A 19900620

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5103819	A		14		

Abstract (Basic): US 5103819 A

The **state machine** provides automatic gain control of sensing functions in an implantable cardiac stimulator. The state controls sensing levels based on **present** sensed **conditions** and on the **prior state** of the heart. Different rates of adjustment are selected under varying conditions so that the gain level for sense amplifiers can be adjusted without significant overshoot.

The **state machine** comprises a set of four conditions or states together with interconnections or logical paths from one state to another. The rate of adjustment of sense amplifier gain is based on the path traversed in the **state machine** so that different effective time constants for the control function may be used for different conditions.

USE/ADVANTAGE - Implantable cardiac stimulators such as pacemakers and defibrillators. Improved response characteristics of automatic gain control so accurate sensing can be maintained.

Dwg.3/9

Title Terms: STATE; MACHINE; CONTROL; CARDIAC; STIMULATING; SELECT; RATE; ADJUST; SO; GAIN; LEVEL; SENSE; AMPLIFY; CAN; ADJUST; SIGNIFICANT; OVERSHOOT

Derwent Class: P34; S05

International Patent Class (Additional): A61N-001/36

File Segment: EPI; EngPI

16/5/16 **(Item 14 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

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009015281 **Image available**

WPI Acc No: 1992-142618/199218

XRPX Acc No: N92-106726

Finite - state machine **for reliable computing and adjustment systems**

- has combinational logic and status memory with comparator for detecting abnormal states and reset signal

Patent Assignee: SGS THOMSON MICROELTRN SRL (SGSA)
Inventor: MOLONEY D; SACCHI F; VAI G; ZUFFADA M
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 482495	A	19920429	EP 91117649	A	19911016	199218	B
EP 482495	A3	19930224	EP 91117649	A	19911016	199348	
IT 1246467	B	19941119	IT 9021816	A	19901022	199516	
US 5426486	A	19960611	US 91779680	A	19911021	199629	N
			US 9342856	A	19930405		
EP 482495	B1	19980708	EP 91117649	A	19911016	199831	
DE 69129727	E	19980813	DE 629727	A	19911016	199838	
			EP 91117649	A	19911016		

Priority Applications (No Type Date): IT 9021816 A 19901022; US 9342856 A 19930405
Cited Patents: No-SR.Pub; 4.Jnl.Ref; JP 1152379; SU 826356
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 482495	A	E	5		
Designated States (Regional): DE FR GB SE					
US 5426486	A		5	G06F-011/30	Cont of application US 91779680
EP 482495	B1	E		G06F-007/00	
Designated States (Regional): DE FR GB SE					
DE 69129727	E			G06F-007/00	Based on patent EP 482495
IT 1246467	B			H03K-000/00	

Abstract (Basic): EP 482495 A

A **Finite - state machine** comprises a combinatorial logic (10) connected to a status memory (11) by means of connections which carry **future state** signals (12) and **current state** signals (13). The combinatorial logic comprises input terminals (14) for external input signals and output terminals (15) for output signals generated by the combinatorial logic.

The **finite - state machine** has circuitry for comparing the **future state** signals to a reference level (16) the comparator can output an error signal (18) to reset the **finite - state machine** and/or the system which includes it.

USE/ADVANTAGE - In critical computing and adjustment systems, detects and resets undesired states.

Dwg.3/5

Title Terms: FINITE; STATE; MACHINE; RELIABILITY; COMPUTATION; ADJUST; SYSTEM; COMBINATION; LOGIC; STATUS; MEMORY; COMPARATOR; DETECT; ABNORMAL; STATE; RESET; SIGNAL
Derwent Class: T01
International Patent Class (Main): G06F-007/00; G06F-011/30; H03K-000/00
International Patent Class (Additional): G06F-011/08
File Segment: EPI

16/5/17 **(Item 15 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

008180016 **Image available**
WPI Acc No: 1990-067017/199009
XRPX Acc No: N90-051525

Channel encoder for generating rotationally invariant trellis codes - generates outputs according to state block where hexagonal constellation has subconstellations which are distinct rotation of each other

Patent Assignee: GENERAL DATACOMM (GEDA-N)
Inventor: COLE P D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4891823	A	19900102	US 88262714	A	19881026	199009	B

Priority Applications (No Type Date): US 88262714 A 19881026
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 4891823 A 12

Abstract (Basic): US 4891823 A

An encoder generates rotationally invariant trellis codes when used with a signal constellation having m subconstellation indexed by j. Each subconstellation has a number of points, where each subconstellation is a distinct rotation by j(360/m) deg. of another subconstellation such that no cubsconstellation has a point in common with another subconstellation. The encoder has a state block and a state update block.

The **state machine** receives q inputs i, and generates m outputs [illegible] pq and where p and q are integers greater than one and [illegible] common factors. Outputs m are generated according to inputs i [illegible] states s of the state block according to j = i mod q and jd = s mod p, where the state block can assume n states, and n = md were d is an integer greater than one and has no common factors with p. The state update block updates the state block to a new **state** t chosen from the **allowable** n **states** based on the output j and **previous state** s according to t = jd + F(s-jd) mod n, where F is the permutation of 0 to n-1 and is a function given by F(am+b)=bd+a=0 to d-1, and for b=0 to m-1.

USE - Generates rotationally invariant trellis codes used with hexagonal constellations which are rotations of each other.

1/3

Title Terms: CHANNEL; ENCODE; GENERATE; ROTATING; INVARIANT; TRELLIS; CODE; GENERATE; OUTPUT; ACCORD; STATE; BLOCK; HEXAGON; DISTINCT; ROTATING
Index Terms/Additional Words: COMMUNICATE
Derwent Class: U21
International Patent Class (Additional): H04B-014/04
File Segment: EPI

16/5/18 **(Item 16 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
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007541242 **Image available**
WPI Acc No: 1988-175174/198825
XRPX Acc No: N88-133843

Interlocked state machines with encoders - uses present state of one machine to determine next state of other machine and vice-versa during non-overlapping clock phases

Patent Assignee: MOTOROLA INC (MOTI)
Inventor: ATWELL W D; LONGWELL M L
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 4749929 A 19880607 US 86945276 A 19861222 198825 B

Priority Applications (No Type Date): US 86945276 A 19861222
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 4749929 A 6

Abstract (Basic): US 4749929 A

Two or more **state machines** are interlocked so that the outputs of one are the inputs of the next, with the outputs of the last being the inputs of the first. Pref. each **state machine** is responsive to a different clock phase, each non-overlapping w.r.t the others. In general, each **state machine** comprises a next state encoder having several inputs and a set of outputs. The set of outputs of the **present state** decoder of the first of the **state machines** are coupled to respective inputs of the next state encoder of the second **state machine** .

The set of outputs of the **present state** decoder of the second **state machine** are coupled to respective inputs of the next state encoder of the third **state machine** , if any, and so on. This continues until the set of outputs of the **present state** decoder of the **last state machine** are coupled to respective inputs of the next state encoder of the first **state machine** .

1/3

Title Terms: INTERLOCKING; STATE; MACHINE; ENCODE; PRESENT; STATE; ONE; MACHINE; DETERMINE; STATE; MACHINE; VICE-VERSA; NON; OVERLAP; CLOCK; PHASE

Derwent Class: T06; U21

International Patent Class (Additional): G05B-011/32

File Segment: EPI

16/5/19 **(Item 17 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

007499088 **Image available**

WPI Acc No: 1988-133021/198819

XRPX Acc No: N88-101096

Asynchronous state machine e.g. for programmable control device - has timing circuit which detects changes in input data and initiates clock pulse applied to gate control of state register

Patent Assignee: TEKTRONIX INC (TEKT)

Inventor: KIRKPATRIC D C

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4740891	A	19880426	US 85730920	A	19850506	198819	B

Priority Applications (No Type Date): US 85730920 A 19850506

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4740891	A		10		

Abstract (Basic): US 4740891 A

The asynchronous **state machine** waits a variable length of time after detecting a change in input stage before initiating a machine state change. The new machine state is a function of the **previous** machine **state** and the input state at the end of the waiting time, thereby allowing multiple, non-simultaneous input changes to occur during the waiting time without initiating intermediate state changes. The waiting time is a function of the current stage of the machine. One state variable of a set characterising the **current state** of the machine indicates whether the **current state** is an intermim state in a sequence of states occurring after an input stage change.

Following a machine state change, this sequencing state variable initiates a subsequent state change, in the absence of any further input stage changes, when the sequencing state variable associated with the **current** machine **state** indicates that the **current** machine **state** is an interim state of a sequence of states.

ADVANTAGE - Time required to change states is minimised

Title Terms: ASYNCHRONOUS; STATE; MACHINE; PROGRAM; CONTROL; DEVICE; TIME; CIRCUIT; DETECT; CHANGE; INPUT; DATA; INITIATE; CLOCK; PULSE; APPLY; GATE ; CONTROL; STATE; REGISTER

Derwent Class: T01; U21

International Patent Class (Additional): G06F-009/00

File Segment: EPI

16/5/20 **(Item 18 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

[illegible]

WPI Acc No: 1987-335041/198747

Related WPI Acc No: 1986-266544; 1993-019837
XRPX Acc No: N87-250817

In-system programmable logic device - has matrix array of switch cells programmable, while isolated from input to connect input and product term lines

Patent Assignee: LATTICE SEMICONDUCTOR CORP (LATT-N)
Inventor: DARLING R D; RUTLEDGE D L; TURNER J E
Number of Countries: 012 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8707071	A	19871119	WO 871099	A	19870512	198747	B
EP 267271	A	19880518	EP 87903607	A	19870512	198820	
JP 63503270	W	19881124	JP 87503184	A	19870512	198902	
US 4855954	A	19890808	US 88262493	A	19881025	198939	
US 4879688	A	19891107	US 88862815	A	19880513	199003	
US 4896296	A	19900123	US 88288945	A	19881223	199011	
EP 267271	B1	19950222	EP 87903607	A	19870512	199512	
			WO 87US1099	A	19870512		
[illegible]	G	19950330	DE 3751084	A	19870512	199518	
			EP 87903607	A	19870512		
			WO 87US1099	A	19870512		

Priority Applications (No Type Date): US 86862815 A 19860513; US 85707662 A 19850304; US 88288945 A 19881223
Cited Patents: US 4441074; US 4532535; US 4617479; US 4625311; 04Jnl.Ref; EP 55348
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8707071	A	E	87		
Designated States (National): JP					
Designated States (Regional): AT BE CH DE FR GB IT LU NL SE					
EP 267271	A	E			
Designated States (Regional): DE FR GB IT					
US 4879688	A		42		
US 4896296	A		41		
EP 267271	B1	E	51	H03K-019/177	Based on patent WO 8707071
Designated States (Regional): DE FR GB IT					
DE 3751084	G			H03K-019/177	Based on patent EP 267271
					Based on patent WO 8707071

Abstract (Basic): WO 8707071 A

A programmable logic device includes an array (10) of floating gate field effect transistors functioning as nonvolatile switches to correct the device input and product term lines in a user assigned manner. During reprogramming, the device normal inputs and outputs are [illegible], and reprogramming data fed to the product term columns of the array via a serial shift register latch (30), array raws being selected via a decoder (20). Loss of present output data may be prevented by latching, or the device outputs tri-stated, during reprogramming.

ADVANTAGE - The device chip is controlled by a **state - machine** to minimise need for additional pins, provides for rapid reprogramming, erasing, and verification function to be carried out while the device is installed in the users systems.

Title Terms: SYSTEM; PROGRAM; LOGIC; DEVICE; MATRIX; ARRAY; SWITCH; CELL; PROGRAM; ISOLATE; INPUT; CONNECT; INPUT; PRODUCT; TERM; LINE
Derwent Class: U13; U14; U21
International Patent Class (Main): H03K-019/177
International Patent Class (Additional): G01R-015/12; G06F-007/00; G06F-011/26; G11C-007/00; G11C-011/34; H03K-019/17
File Segment: EPI

16/5/21 **(Item 19 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

004524739
WPI Acc No: 1986-028083/198604

XRPX Acc No: N86-020532
Symbol coding appts. for band-limited channel modulated transmission - delivers corresp. signal selected from one of many subsets at least two of which have common available signal
Patent Assignee: CODEX SA (RENI)
Inventor: FORNEY G D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4562426	A	19851231	US 82439740	A	19821108	198604	B

Priority Applications (No Type Date): US 82439740 A 19821108
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4562426	A		12		

Abstract (Basic): US 4562426 A

A **finite - state** device occupies, at any given time one state from among a finite number of possible states, the one state depending on previously sent symbols. Each possible transition from a **previous state** to a **current state** is associated with a subset of alphabet signals. Signal selection logic receives each symbol to be sent and a **current state** from the **finite state** device.

The logic delivers a corresp. signal selected from one subset among a number of subsets whose respective members are such that at least two of the subsets have at least one available signal in common and at least one available signal belongs to only one subset. A carrier is modulated in accordance with the delivered signal.

ADVANTAGE - Achieves coding gain with relatively small increase in alphabet size

Title Terms: SYMBOL; CODE; APPARATUS; BAND; LIMIT; CHANNEL; MODULATE; TRANSMISSION; DELIVER; CORRESPOND; SIGNAL; SELECT; ONE; SUBSET; TWO; COMMON; AVAILABLE; SIGNAL
Derwent Class: U21; W01
International Patent Class (Additional): H03K-013/24
File Segment: EPI

16/5/22 **(Item 20 from file: 350)**
File 350:Derwent WPIX

WPI Acc No: 1985-147736/198525
XRPX Acc No: N85-111464
Space saving structure for dynamic programmable logic array - has AND and OR planes folded together with all transistors orientated in same direction
Patent Assignee: GEN INSTR CORP (GENN)
Inventor: CARTER T M; SMITH K F
Number of Countries: 007 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 144635	A	19850619	EP 84112363	A	19841013	198525	B
JP 60103829	A	19850608	JP 84218784	A	19841019	198529	
US 4683012	A	19860415	US 83543956	A	19831020	198618	
EP 144635	B	19900613				199024	
DE 3482535	G	19900719				199030	

Priority Applications (No Type Date): US 83543956 A 19831020
Cited Patents: 1.Jnl.Ref; EP 109125
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 144635	A	E	26		
Designated States (Regional): BE DE FR GB IT					
EP 144635	B				
Designated States (Regional): BE DE FR GB IT					

Abstract (Basic): EP 144635 A

The array includes a number of AND rows (Ro,Rn) with transistors (300,302) for precharging the AND rows to one logic level (VDD). An additional row (Ra) is provided along a transistor to allow precharging of the row to another logic level (ground). The array includes a series of data columsn (316,318,320) and an output column (328) coupled to the AND row (Ro).

A number of logic cells (306,308) are divided among the AND rows. Each cell has an input terminal coupled to the data column (316,318), an output connected to one AND row, and a second output connected to the next successive AND row. The AND conditions of signals on the data columns are formed on the AND rows (Ro,Rn), and the OR condition of the AND rows is formed on the output column.

ADVANTAGE - Provides dynamic compact array.

32/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05616451 **Image available**
STATE ASSIGNMENT METHOD AND DEVICE FOR **FINITE STATE MACHINE**

PUB. NO.: 09-231251 [JP 9231251 A]
PUBLISHED: September 05, 1997 (19970905)
INVENTOR(s): MATSUNAGA TAEKO
MATSUNAGA YUSUKE
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-034750 [JP 9634750]
FILED: February 22, 1996 (19960222)
INTL CLASS: [6] G06F-017/50; H01L-021/82
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications); 42.2 (ELECTRONICS -- Solid State Components)
JAPIO KEYWORD: R129 (ELECTRONIC MATERIALS -- Super High Density Integrated Circuits, LSI & GS

ABSTRACT

PROBLEM TO BE SOLVED: To accurately evaluate a state assignment solution and to improve this solution in sequence by deciding an index showing the scale of a combinational logic circuit based on a logical expression produced in the state transition description and the state assignment solution and then applying the index for evaluation of the state assignment solution.

SOLUTION: A binary code is assigned to every state when a **finite state machine** consisting of a state memory circuit and a combinational logic circuit is synthesized from the state transition description. An analysis means 111 analyzes the state transition description to produce a logical expression showing a combinational logic circuit that constructs the **finite state machine** . An evaluation means 112 simplifies the logical expression by means of a state assignment solution in response to the input of the state assignment solution that **secures** the correspondence between the binary codes and the states. Then the means 112 evaluates the scale of the combinational logic circuit based on the simplified logical expression. An improvement processing means 113 decides whether the state assignment solution can be improved based on the evaluation result of the scale of the combinational logic circuit. If the state assignment solution can be improved, a new state assignment solution is generated and used for the evaluation processing.

32/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

01778360 **Image available**
LOGICAL INTEGRATION CIRCUIT

PUB. NO.: 60-256860 [JP 60256860 A]
PUBLISHED: December 18, 1985 (19851218)
INVENTOR(s): FUNABASHI TSUNEO
IWASAKI KAZUHIKO
YAMAGUCHI NOBORU
SHIMURA TAKANORI
TATEZAKI JIYUNICHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-110731 [JP 84110731]
FILED: June 01, 1984 (19840601)
INTL CLASS: [4] G06F-013/12; G06F-003/06
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units); 45.3 (INFORMATION PROCESSING -- Input Output Units)
JOURNAL: Section: P, Section No. 457, Vol. 10, No. 135, Pg. 66, May

20, 1986 (19860520)

ABSTRACT

[illegible]: To obtain an LSI structure that can be applied to the design of a [illegible] of an external input/output device having high performance and a high function, by forming a hierarchical processor within an LSI and mapping an ROM and a **finite state** transition machine to host and subordinate processors respectively.

CONSTITUTION: The control function of an external input/output device 201 for common application is shared and executed by >=1 **state machines** FSM. An FSM1 which performs reception control on a transmission clock .psi.'. When data are transferred between a host system and the device 201, a data buffer 204 is provided in a control LSI in case the transfer speeds are different between the hose system and the device 201 or the time is needed for preparation of data transfer. Furthermore, a connection port of the FSM is standardized since the FSM can be added for each control function of the device 201. A microprogram controller .mu.C has a function to allocate the start sequence. Thus an on-chip hierarchical processor structure is **secured** to define the .mu.C and the FSM as the host and subordinate processors respectively.

32/5/3 **(Item 1 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

015340542 **Image available**
WPI Acc No: 2003-401480/200338
Related WPI Acc No: 2002-499109; 2003-017000; 2003-238047; 2003-392445; 2003-492296
XRPX Acc No: N03-320173
Factoring method for ambiguous finite - state **transducer, involves copying arc of fully unfolded-state transducer to unambiguous and fail** safe finite - state **transducers while replacing symbols with diacritic when arc is inside ambiguity field**
Patent Assignee: XEROX CORP (XERO)
Inventor: KEMPE A
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030004705	A1	20030102	US 2000194493	P	20000403	200338	B
			US 2000737552	A	20001218		

Priority Applications (No Type Date): US 2000194493 P 20000403; US 2000737552 A 20001218
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030004705	A1		63	G06F-017/27	Provisional application US 2000194493

Abstract (Basic): US 20030004705 A1

NOVELTY - The method involves preprocessing the ambiguous **finite - state** transducer (FST) to create a fully-unfolded FST having states and arcs. The arc is copied to the unambiguous and fail **safe** FSTs while replacing the corresponding output and input symbols with the diacritic, when the arc is inside an ambiguity field.

DETAILED DESCRIPTION - The arc is copied to the unambiguous and fail **safe** FSTs while replacing the corresponding input symbol with the corresponding output symbol, when the arc is outside the ambiguity field. An INDEPENDENT CLAIM is also included for an apparatus for factoring an ambiguous **finite - state** transducer into an unambiguous **finite - state** transducer and a fail **safe finite - state** transducer.

USE - Used for factoring an ambiguous **finite - state** transducer into an unambiguous **finite - state** transducer and a fail **safe finite - state** transducer.

ADVANTAGE - Enables efficient processing of input strings by lexical transducers.

DESCRIPTION OF DRAWING(S) - The figure shows an example of a simple **finite state** automation.
pp; 63 DwgNo 1/76
Title Terms: METHOD; AMBIGUOUS; FINITE; STATE; TRANSDUCER; COPY; ARC; UNFOLD; STATE; TRANSDUCER; UNAMBIGUOUS; FAIL; **SAFE** ; FINITE; STATE; TRANSDUCER; REPLACE; SYMBOL; ARC; AMBIGUOUS; FIELD
Derwent Class: T01
International Patent Class (Main): G06F-017/27
File Segment: EPI

32/5/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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Image available
WPI Acc No: 2003-301365/200329
XRPX Acc No: N03-239734
Method for transmitting large volumes of data via an asynchronous interface in a checker-master type redundancy circuit relies on data type and volume to be transmitted in accordance with different transmission cycles.
Patent Assignee: SIEMENS AG (SIEI)
Inventor: HECHFELLNER F; VETTER R
Number of Countries: 025 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
WO 200326175 A2 20030327 WO 2002DE3155 A 20020828 200329 B

Priority Applications (No Type Date): DE 1042611 A 20010831
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
WO 200326175 A2 G 14 H04J-003/00
Designated States (National): CN US
Designated States (Regional): AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LU MC NL PT SE SK TR

Abstract (Basic): WO 200326175 A2
NOVELTY - Data is transmitted by relying on data type and volume to be transmitted in accordance with different transmission cycles.
Finite - **state machines** (FSMs) determine the course of operations on both sides of an interface. The FSMs can control the transfer of data via any number of data buses of any size. On each data bus data is kept stable on the output side until it can be **securely** transferred on the input side.
USE - None given.
ADVANTAGE - Any number of data items are transmitted with each sequential phase until a cycle is completed.
DESCRIPTION OF DRAWING(S) - The drawing shows a circuit diagram for parallel data transmission via an asynchronous interface according to the master-checker redundancy principle.
pp; 14 DwgNo 1/2
Title Terms: METHOD; TRANSMIT; VOLUME; DATA; ASYNCHRONOUS; INTERFACE; CHECK ; MASTER; TYPE; REDUNDANT; CIRCUIT; RELY; DATA; TYPE; VOLUME; TRANSMIT; ACCORD; TRANSMISSION; CYCLE
Derwent Class: T01; W01; W02
International Patent Class (Main): H04J-003/00
File Segment: EPI

32/5/5 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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Image available
WPI Acc No: 2002-722209/200278
XRPX Acc No: N02-569462
Memory controlling method for laptop computer, involves switching

functionality to assert chip select signal within memory request to finite state machine , if cycle is row or page miss

Patent Assignee: INTEL CORP (ITLC)
Inventor: FREKER D E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6442645	B1	20020827	US 98205447	A	19981204	200278	B

Priority Applications (No Type Date): US 98205447 A 19981204
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6442645	B1		19	G06F-012/00	

Abstract (Basic): US 6442645 B1

NOVELTY - A memory request is partially decoded and the **safe** indicator signals are sampled. A logic block based on the decoding result, indicator signals, determines whether it is **safe** to issue a chip select and if so asserts the chip select. The functionality of chip assert is switched to a **finite state machine** , if the cycle type of memory request is a page or row miss.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Memory controller;

(2) Memory controlling system; and

(3) Machine-readable medium storing memory control program.

USE - For controlling memory e.g. SDRAM in laptop, desktop, palmtop, server, mainframe computers, printer, plotter, scanner, facsimile, automatic teller machine, wireless communication equipment.

ADVANTAGE - Effectively reduces latency of a cycle initiated by a bus-mastering agent to memory. Also, improves the performance of write cycles, allowing them to be completed with minimal latency, freeing the memory interface for other cycles. Thus, provides a performance boost for memory intensive applications.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart illustrating memory controlling process.

pp; 19 DwgNo 5C/6

Title Terms: MEMORY; CONTROL; METHOD; COMPUTER; SWITCH; FUNCTION; CHIP; SELECT; SIGNAL; MEMORY; REQUEST; FINITE; STATE; MACHINE; CYCLE; ROW; PAGE ; MISS
Derwent Class: T01; T05
International Patent Class (Main): G06F-012/00
File Segment: EPI

32/5/6 **(Item 4 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

Image available
API Acc No: 2001-060796/200107
XRPX Acc No: N01-045583

Chip card system for electronic transaction, has transaction control application module for checking authentication **of electronic card before transaction**

Patent Assignee: KONINK KPN NV (NEPO)
Inventor: FRANSEN F
Number of Countries: 090 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200063856	A1	20001026	WO 2000EP2853	A	20000331	200107	B
NL 1011790	C2	20001017	NL 991011790	A	19990414	200107	
AU 200042922	A	20001102	AU 200042922	A	20000331	200107	

Priority Applications (No Type Date): NL 991011790 A 19990414
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200063856	A1	E	10	G07F-007/10	

Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN
CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP
KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE
SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR
IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW

NL 1011790 C2 G07F-007/10
AU 200042922 A G07F-007/10 Based on patent WO 200063856

Abstract (Basic): WO 200063856 A1

NOVELTY - Chip card system has transaction control application module (TCAM) (3) for checking **authentication** of electronic card before transaction.

USE - Chip card system for electronic transaction such as electronic purse payment or ticketing transaction.

ADVANTAGE - By checking **authentication** of card, proof about characteristic of issued chip card can be confirmed.

DESCRIPTION OF DRAWING(S) - The figure shows the **finite state machine** for stepwise checking and control of electronic transaction.

Transaction control application module (3)

pp; 10 DwgNo 2/2

Title Terms: CHIP; CARD; SYSTEM; ELECTRONIC; TRANSACTION; TRANSACTION; CONTROL; APPLY; MODULE; CHECK; AUTHENTICITY; ELECTRONIC; CARD; TRANSACTION

Derwent Class: T05

International Patent Class (Main): G07F-007/10

File Segment: EPI

32/5/7 **(Item 5 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

012812617 **Image available**

WPI Acc No: 1999-618848/199953

XRPX Acc No: N99-456219

Computer personality module for use in multimedia computers

Patent Assignee: MATSUSHITA ELECTRIC IND CO LTD (MATU)

Inventor: HATA K; KIBRE N; SHAW R; TERADA Y

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5966691	A	19991012	US 97841043	A	19970429	199953	B

Priority Applications (No Type Date): US 97841043 A 19970429

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5966691	A		8	G10L-005/02	

Abstract (Basic): US 5966691 A

NOVELTY - A **finite state** grammar of message assembler (18) defines **finite state** slots for insertion of words to construct event notification message. A pseudo-random word generator selects and places words in slots to vary text of message for a predetermined condition.

DETAILED DESCRIPTION - An event handler (14) responds to operating system and application program for generating event notification messages in response to predetermined conditions. A message assembler of personality module is receptive to event notification messages for assembling text strings which correspond to the messages. A text-to-speech engine (22) is receptive of text strings for generating speech messages corresponding to text strings.

USE - For providing pseudo-randomly varied speech messages in multimedia computers.

ADVANTAGE - The personality module produces simulated computer personality which handles screen saver functions containing **security** functions and provides useful spoken messages matching computer's operating context.

DESCRIPTION OF DRAWING(S) - The figure shows system block diagram of screen saver and message notification system.
Event handler (14)
Message assembler (18)
Text-to- speech engine (22)
pp; 8 DwgNo 1/2
Title Terms: COMPUTER; PERSON; MODULE; COMPUTER
Derwent Class: P86; T01; W04
International Patent Class (Main): G10L-005/02
File Segment: EPI; EngPI

32/5/8 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012431035 **Image available**
WPI Acc No: 1999-237143/199920
XRPX Acc No: N99-176415
Transit control system for automatic guided vehicle - has several finite state machines **which are operated in predetermined priority level order of control performed for various transit characteristics**
Patent Assignee: FUJITSU LTD (FUIT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 11065654	A	19990309	JP 97215365	A	19970811	199920	B

Priority Applications (No Type Date): JP 97215365 A 19970811
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11065654	A		8	G05D-001/02	

Abstract (Basic): JP 11065654 A
NOVELTY - Several **finite state machines** are provided for control of transit characteristics. The machines are operated in a predetermined priority level order of control performed for detection and removal of obstruction, position error correction on TWY detection, reverse direction drive and reduction of attitude angle deviation of vertical shaft periphery to TWY, on detaching TWY.
USE - For automatic guided vehicle running along TWY such as magnetic TWY.
ADVANTAGE - **Secures** simplified real time operation, thus avoiding collision with other vehicles. Reduces development cost as simple algorithm is used. DESCRIPTION OF DRAWING(S) - The figure shows the conceptual diagram of transit control system.
Dwg.1/7
Title Terms: TRANSIT; CONTROL; SYSTEM; AUTOMATIC; GUIDE; VEHICLE; FINITE; STATE; MACHINE; OPERATE; PREDETERMINED; PRIORITY; LEVEL; ORDER; CONTROL; PERFORMANCE; VARIOUS; TRANSIT; CHARACTERISTIC
Derwent Class: S02; T06; W06
International Patent Class (Main): G05D-001/02
File Segment: EPI

32/5/9 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010784214 **Image available**
WPI Acc No: 1995-185473/199524
XRPX Acc No: N95-145257
Data communications network security **system e.g. for protection against computer virus - uses adaptable simultaneously parallel array of** finite state machines **to monitor generated** security **threat patterns**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: HERSHEY P C; JOHNSON D B; LE A V; MATYAS S M; WACLAWSKY J G; WILKINS J D

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5414833	A	19950509	US 93144161	A	19931027	199524	B

Priority Applications (No Type Date): US 93144161 A 19931027
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5414833	A		44	H04L-009/00	

Abstract (Basic): US 5414833 A

The **security** system includes a **finite state machine** with a memory, an address register which is coupled to the network and a start signal input and **security** threat pattern detection output which are coupled to a counter. The memory stores a **finite state machine** definition used for detecting a data **security** threat pattern. Similar second and third **state machines** are coupled with the first **state machine** by a programmable interconnection arrangement which selectively interconnects the first **security** threat pattern detection output to the second or third start signal inputs.

The inputs of a **security** event vector assembly device are coupled to all three counters, and a **security** event vector is assembled from the accumulated count value in the first counter and the second or third counters and represents the number of occurrences of the first and second or third **security** threat patterns on the network. A responder (300) with an input coupled to the **security** event vector assembly device, has outputs coupled to the first, second and third **state machine** memories and the programmable interconnection device. The responder changes the data **security** threat patterns to be detected on the network.

ADVANTAGE - Real time detection of transmitted, infected programs and data. Adaptive **state machine** monitor can be dynamically reprogrammed.

Dwg.6/24

Title Terms: DATA; COMMUNICATE; NETWORK; **SECURE** ; SYSTEM; PROTECT; COMPUTER; VIRUS; ADAPT; SIMULTANEOUS; PARALLEL; ARRAY; FINITE; STATE; MACHINE; MONITOR; GENERATE; **SECURE** ; THREAT; PATTERN
Derwent Class: T01; W01
International Patent Class (Main): H04L-009/00
File Segment: EPI

32/5/10 (Item 8 from file: 350)
File 350:Derwent WPIX

430 **Image available**
WPI Acc No: 1994-170346/199421
XRPX Acc No: N94-134183

Financial document and cheque processing and printing system - has electronic lock for incrementing counter each time system is accessed, and sending interrupt signal to database and networking controller, which checks counter reading when system is next powered up

Patent Assignee: TRI-PLUS TECHNOLOGY CORP (TRIP-N)
Inventor: LU J
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2273375	A	19940615	GB 9225616	A	19921208	199421	B
CN 1093186	A	19941005	CN 93103562	A	19930329	199717	N
GB 2273375	B	19970521	GB 9225616	A	19921208	199723	

Priority Applications (No Type Date): GB 9225616 A 19921208; CN 93103562 A 19930329
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2273375	A		38	G06F-015/21	
CN 1093186	A			G06F-015/20	

GB 2273375 B G06F-017/60

Abstract (Basic): GB 2273375 A

The system serves as a workstation with financial **security** and networking capabilities under software control. The system supports financial document typesetting, printing, data processing and data management, and comprises a control module, an operation module and a database. The control module comprises a high speed laser printer (10), a database/networking controller (11), a synchronous power supply (12), an electronic lock (13), a system real-time recorder (14), an authorisation card (15), an account identification card (16), and a removable high capacity storage device (17).

The operation module comprises a display (20), an operation processor (21), a financial keyboard (22), an optical scanner (23), and a magnetic ink character reader/magnetic reader (24). The control software is based on a **finite state machine** . The system may be extended by using several control modules and operation modules.

ADVANTAGE - Automatically prints and processes documents. Supports various system task applications, English/Chinese characters, complete printing capability, management of cheque, bill, bond etc., networking, off-line, uninterrupted power supply, keeping of blank cheques, automatic MICR recording function, high reliability and high **security** .

Dwg.2/11

Title Terms: FINANCIAL; DOCUMENT; CHEQUE; PROCESS; PRINT; SYSTEM; ELECTRONIC; LOCK; INCREMENT; COUNTER; TIME; SYSTEM; ACCESS; SEND; INTERRUPT; SIGNAL; DATABASE; CONTROL; CHECK; COUNTER; READ; SYSTEM; POWER ; UP

Derwent Class: T01; T04; T05

International Patent Class (Main): G06F-015/20; G06F-015/21; G06F-017/60

International Patent Class (Additional): G06K-015/00; G07F-019/00

File Segment: EPI

32/5/11 **(Item 9 from file: 350)**

image available

WPI Acc No: 1991-178273/199124

XRPIX Acc No: N91-136520

Point of sale system - includes two levels of processor nodes with each processor having transaction file and router-schedule software

Patent Assignee: VIATA CORP (VIAT-N)

Inventor: CARROLL M R; MILLS D G; SMALL J A

Number of Countries: 024 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9107725	A	19910530				199124	B
AU 9169035	A	19910613				199137	

Priority Applications (No Type Date): US 89439981 A 19891121

Cited Patents: NoSR.Pub

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9107725	A				

Designated States (National): AU BR CA FI HU JP KP KR NO RO SU

Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LU NL SE

Abstract (Basic): WO 9107725 A

The RPSOH processor includes a master transaction screening database, and facilities for maintaining up-to-date screening data and complete transaction data in all PSOP's; the point of sale/use system also includes Point of Sale Terminals (PSOT's), each one having an assigned identification code. These PSOT's are connected in parallel to a suitable standard port of the associated PSOP. Each processor comprises a **finite state** software operating system controller, termed a router/scheduler, which is adapted to implement the specific tasks assigned to a processor, as well as manages all of the hardware and

software resources of a processor in accordance with a defined priority plan for ordering task execution.

Each PSOP has a complete transaction file, which includes transactions processed by other PSOP's, and making it possible to generate consolidated transaction reports at a terminal of each PSOP. The primary task assigned to a RPOSH is to establish frequent communication with the PSOP's for the purpose of sending up-to-date screening and transaction data to each PSOP.

USE/ADVANTAGE - Commercial transactions applications, banking, insurance, shipping etc. Improved Point of Sale Processing system with enhanced effectiveness, better operating characteristics, greater **security** and reduced cost. (86pp Dwg.No.1/16)

Title Terms: POINT; SALE; SYSTEM; TWO; LEVEL; PROCESSOR; NODE; PROCESSOR; TRANSACTION; FILE; ROUTER; SCHEDULE; SOFTWARE
Derwent Class: T01; T05
International Patent Class (Additional): G06F-015/24
File Segment: EPI

32/5/12 **(Item 10 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
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004057355
WPI Acc No: 1984-202896/198433
XRPX Acc No: N84-151641

Run length limited coded data stream generation method - transferring source data stream over several parallel channels to NRZ detector with each channel encoding its input data

Patent Assignee: IBM CORP (IBMC)
Inventor: SIEGEL P H; TODD S J
Number of Countries: 005 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 116020	A	19840815	EP 84850003	A	19840103	198433	B
JP 59141854	A	19840814	JP 83238029	A	19831219	198438	
US 4567464	A	19860128	US 83461842	A	19830128	198607	

Priority Applications (No Type Date): US 83461842 A 19830128
Cited Patents: 1.Jnl.Ref; EP 71680; US 3689899; US 4028535; US 4122440; US 4286256
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 116020	A	E	53		

Designated States (Regional): DE FR GB

Abstract (Basic): EP 116020 A

The appts. has several 'k' run length limited encoders for interleave encoding a data bit stream applied over a path. Several of k run length limited (RLL) decoders for separate and decode an interleaved RLL bit stream. The method involves transferring the source data stream over the k parallel channel encoders to a non-return to zero (NRZ) detector. Each channel encodes its input data into an RLL stream with a frequency spectrum notched at f/n HZ, where f is a bit rate and n is a positive integer.

The encoded RLL streams from all the channels are k-way interleaved into the NRZ detector such that the merged NRZ stream exhibits a notch at f/kn HZ.

USE - For recording data on a magnetic tape or disc.

35/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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06621237 **Image available**
PREBOOT **SECURITY** **CONTROLLER**

PUB. NO.: 2000-207048 [JP 2000207048 A]
PUBLISHED: July 28, 2000 (20000728)
INVENTOR(s): HUANG JUNG-CHIH
OH BRIAN
HUANG YISHAO MAX
REYNOSO AARON
DU STERLING
APPLICANT(s): O 2 MICRO INC
APPL. NO.: 11-352172 [JP 99352172]
FILED: November 05, 1999 (19991105)
PRIORITY: 107995 [US 98107995], US (United States of America), November 11, 1998 (19981111)
121643 [US 99121643], US (United States of America), February 24, 1999 (19990224)
INTL CLASS: G06F-001/00; G06F-009/06; G06F-012/14

ABSTRACT

PROBLEM TO BE SOLVED: To allow a digital logic circuit to disable an information processor by comparing a password that an input circuit receives with a user password in **security** operation mode, and sending it a power subsystem and exciting the operation of a digital computer when the passwords match each other.

SOLUTION: The password input circuit 82 is connected to a 4-button type **security** key pad by a key pad bus 84, the user of an electronic device presents a password to a **state machine** 52, and the password is compared with one or more passwords registered in a flash memory 56. Then when the **security controller** 42 enters the **security** operation mode, its passwords match each other, its output signal is sent to the power subsystem, and the operation of the digital computer is excited.

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35/5/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013159447 **Image available**
WPI Acc No: 2000-331320/200029
XRPX Acc No: N00-249514
Pre-boot security controller **adapted for inclusion in electronic digital computer and its power subsystem; energizes operation of computer if password received by password input circuit matches user passwords recorded in memory**
Patent Assignee: 02 MICRO INT LTD (ZERO-N)
Inventor: DU S; HUANG J; HUANG Y M; OH B; REYNOSO A
Number of Countries: 027 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1001331	A2	20000517	EP 99308752	A	19991103	200029	B
JP 2000207048	A	20000728	JP 99352172	A	19991105	200041	
TW 436677	A	20010528	TW 99119638	A	19991118	200172	

Priority Applications (No Type Date): US 99121643 P 19990224; US 98107995 P

Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
EP 1001331 A2 E 11 G06F-001/00
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

[illegible] A 11 G06F-001/00
[illegible] G06F-001/00

[illegible] Basic: EP 1001331 A2
[illegible]LITY - An output control (62) is coupled a **state machine** [illegible] for transmitting an output signal to a power subsystem that enables the power subsystem. That may energize operation of the digital computer if the password received by the password input circuit (82) matches a user passwords recorded in the password memory (56).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for:
(a) an electronic device
USE - As a **security** protection for computers and other microprocessor controlled devices for preventing the unauthorized use of such devices.
ADVANTAGE - Disables an information processing appliance, such as a portable, laptop or notebook personal computer, so it becomes inoperable until unlocked by its authorized user, thus discouraging theft and enhances **security** .
DESCRIPTION OF DRAWING(S) - The drawing is a block diagram illustrating in greater detail the pre-boot **security controller** of the present invention.
state machine (52)
password memory (56)
output control (62)
password input circuit (82)
pp; 11 DwgNo 2/2
Title Terms: PRE; BOOT; **SECURE** ; CONTROL; ADAPT; INCLUSION; ELECTRONIC; [illegible]IGITAL; COMPUTER; POWER; SUBSYSTEM; OPERATE; COMPUTER; PASSWORD; RECEIVE ; [illegible]ASSWORD; INPUT; CIRCUIT; MATCH; USER; PASSWORD; RECORD; MEMORY
[illegible] Class: T01
International Patent Class (Main): G06F-001/00
International Patent Class (Additional): G06F-009/06; G06F-012/14
File Segment: EPI

35/5/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012437714 **Image available**
WPI Acc No: 1999-243822/199920
XRPX Acc No: N99-181435
Dual optical transceiver for high bandwidth full duplex communications
Patent Assignee: FINISAR CORP (FINI-N)
Inventor: FREEMAN W R; KANE D S; LEVINSON F H; VU M Q
Number of Countries: 020 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9913601	A1	19990318	WO 98US17870	A	19980828	199920	B
US 5956168	A	19990921	US 97911127	A	19970814	199945	
			US 97924852	A	19970905		

Priority Applications (No Type Date): US 97924852 A 19970905; US 97911127 A 19970814
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
[illegible]	A1	E	30	H04B-010/00	

[illegible]signated States (National): JP
[illegible]signated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

US 5956168	A	H04B-010/00	CIP of application US 97911127

Abstract (Basic): WO 9913601 A1
NOVELTY - A **controller** is coupled to a laser transmitter and a receiver. It has a multi-protocol **state machine** to establish a full duplex connection whenever the other device operates in compliance with a set on-off-on signaling protocol and also with a second set signaling protocol.

USE - The transceiver is used for high bandwidth full duplex communications, particularly open fiber control protocol (OFC protocol).

ADVANTAGE - The module is compatible with both OFC compliant modules and standard modules. Meets the **safety** class 1 product standard irrespective of the connection at the other end of the dual fiber channel.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of a dual optical fiber communication system incorporating a multi-protocol communication module.

pp; 30 DwgNo 2/6

Title Terms: DUAL; OPTICAL; TRANSCEIVER; HIGH; BANDWIDTH; FULL; DUPLEX; COMMUNICATE

Derwent Class: W02

International Patent Class (Main): H04B-010/00

File Segment: EPI

35/5/4 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

010062374 **Image available**

WPI Acc No: 1996-259329/199626

XRPX Acc No: N96-218214

Airport surface safety logic system - uses target state machine to determine position, velocity etc. of aircraft and state of aircraft, whether landing, departing etc., using prediction engine to predict path of each aircraft and thus detecting possible collisions and alerting

Patent Assignee: MASSACHUSETTS INST TECHNOLOGY (MASI)

Inventor: EGGERT J R; KASTNER M P; MORIN T J; STURDY J L; WILHELMSEN H

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5519618	A	19960521	US 93101552	A	19930802	199626	B
			US 95416441	A	19950403		

Priority Applications (No Type Date): US 93101552 A 19930802; US 95416441 A 19950403

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5519618	A		75	B64F-001/22	Cont of application US 93101552

Abstract (Basic): US 5519618 A

The airport **safety** logic system has a target **state machine** receives a number of tracks, each of which includes velocity, acceleration, size, position etc. information about an airport target object i.e. aircraft and also determines, for each track, a state of the aircraft, whether it is stopped, taxi-ing, arriving, landing, aborting a landing, departing, or aborting a departure.

A prediction engine uses the position and velocity information to predict a max. and a min. distance the aircraft could travel in a period of time and determines, if the state of the object is ''arriving,'' whether the aircraft can land on a particular runway of the airport. This prediction logic is the basis for the light-control logic controlling runway-status lights of the airport. An alert logic determines if there is risk of collision based on the prediction logic and if there is, alerts the control tower both visually and audibly.

ADVANTAGE - Provides fully automated airport **safety** control system providing information to **controllers** and pilots and effectively predicts and prevents aircraft collisions.

Dwg.13/20

Title Terms: AIRPORT; SURFACE; **SAFETY** ; LOGIC; SYSTEM; TARGET; STATE; MACHINE; DETERMINE; POSITION; VELOCITY; AIRCRAFT; STATE; AIRCRAFT; LANDING; DEPART; PREDICT; ENGINE; PREDICT; PATH; AIRCRAFT; DETECT; POSSIBILITY; COLLIDE; ALERT

Derwent Class: Q25; T01; W06

International Patent Class (Main): B64F-001/22

File Segment: EPI; EngPI

35/5/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010362462 **Image available**
WPI Acc No: 1995-295885/199539
XRPX Acc No: N95-224136
Architecture of computer program for vehicle diagnosis system - has breakdown code module stored in memory unit
Patent Assignee: FORD MOTOR CO (FORD); FORD GLOBAL TECHNOLOGIES INC (FORD)
Inventor: ARMITAGE J F; FERCH E B; SMITH P F
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7190897	A	19950728	JP 9466267	A	19940404	199539	B
US 5671141	A	19970923	US 9343192	A	19930405	199744	
JP 3394810	B2	20030407	JP 9466267	A	19940404	200324	

Priority Applications (No Type Date): US 9343192 A 19930405
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7190897	A		20	G01M-017/007	
US 5671141	A		22	G01M-015/00	
JP 3394810	B2		19	G01M-017/007	Previous Publ. patent JP 7190897

Abstract (Basic): JP 7190897 A
The computer program is stored in RAM and ROM of a computer. The computer program installs numerous monitor modules which monitor each individual component or a number of component systems of the vehicle and detects the breakdown of the component. The monitor module generates a breakdown subroutine call when it detects a breakdown. Interface is done between the monitor modules and the execution program modules to control the order of enable of monitor module to execution program module.
The monitor modules execute the indicating defect light control and breakdown code storage strategy. A diagnosis scheduler module is executed as a limitation **state machine** . The diagnosis scheduler module controls the sequence and the instruction type self-diagnosis test operated by the monitor module and adjusts it simultaneously to issue store code subroutine call. The indicating defect light **controller** module responds to the store code subroutine call to turn-off or turn-on four independent lights. The computer program executes storage and detection of breakdown code.
ADVANTAGE - Low emission of toxic material from car. Provides precision control of engine and transmission system. **Secures** actuator and sensor operation appropriately. Executes system check. Controls indicating defect light.
Dwg.1/13
Title Terms: ARCHITECTURE; COMPUTER; PROGRAM; VEHICLE; DIAGNOSE; SYSTEM; BREAKDOWN; CODE; MODULE; STORAGE; MEMORY; UNIT
Derwent Class: Q17; S02; T01; X22
International Patent Class (Main): G01M-015/00; G01M-017/007
International Patent Class (Additional): B60R-016/02
File Segment: EPI; EngPI

35/5/6 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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010362462 **Image available**
WPI Acc No: 1995-263776/199534
XRPX Acc No: N95-202779
Computer modelling and evaluation of automobile air bag appts. - constructing inflator state machine **including slots for receiving and**

holding signals corresp. to gas and heat transfer dynamics, and creating model using data for dimensions, chemical compsn., layout etc.

Patent Assignee: THIOKOL CORP (THIO)
Inventor: ROZANSKI J D
Number of Countries: 060 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9519277	A2	19950720	WO 95US28	A	19950104	199534	B
US 5452210	A	19950919	US 94179727	A	19940110	199543	
AU 9514478	A	19950801	AU 9514478	A	19950104	199546	
WO 9519277	A3	19950831	WO 95US28	A	19950104	199619	

Priority Applications (No Type Date): US 94179727 A 19940110
Cited Patents: No-SR.Pub; 1.Jnl.Ref; US 4064392; US 4393013; US 4436674; US 4977529; US 5201581; US 5203205
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9519277	A2	E	43	B60R-000/00	

Designated States (National): AM AT AU BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU JP KE KG KP KR KZ LK LR LT LU LV MD MG MN MW MX NL NO NZ PL PT RO RU SD SE SI SK TJ TT UA UZ VN
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT KE LU MC MW NL OA PT SD SE SZ

[illegible]	A	17	G01N-025/22	
[illegible]	A		B60R-021/16	Based on patent WO 9519277
[illegible]	A3		B60R-000/00	

[illegible] (Basic): WO 9519277 A

A computer model of an air bag inflator is established in which the initial state of components is prepared with details of their dimensions, chemical compsn., disposition and layout.

Consideration is given to components such as combustion chamber (14), ports (16,20), diffusion chamber (18), tank (22) and their possible contents such as combustion pills (36), flow deflector and screen pack (22,40,44). The state of components at times from ignition are determined.

USE/ADVANTAGE - Different designs of gas generator can be evaluated and compared before embarking on actual mfr. and testing. Minimises fabrication testing and avoid destructive testing of gas generating compounds.

Dwg.2/5

Title Terms: COMPUTER; MODEL; EVALUATE; AUTOMOBILE; AIR; BAG; APPARATUS; CONSTRUCTION; INFLATE; STATE; MACHINE; SLOT; RECEIVE; HOLD; SIGNAL; CORRESPOND; GAS; HEAT; TRANSFER; DYNAMIC; MODEL; DATA; DIMENSION; CHEMICAL; COMPOSITION; LAYOUT
Derwent Class: Q17; T01; X22
International Patent Class (Main): B60R-021/16; G01N-025/22
International Patent Class (Additional): G01N-007/02
File Segment: EPI; EngPI

35/5/7 **(Item 6 from file: 350)**
[illegible] File 350:Derwent WPIX
[illegible] Thomson Derwent. All rts. reserv.

009131804 **Image available**
WPI Acc No: 1992-259243/199231
XRPX Acc No: N92-197789

Cellular car telephone dialling controller **- has numerals sequentially heard by user at each dialling step with operator switch closed to dial number when correct number heard**

Patent Assignee: KUNSTADT G H (KUNS-I)
Inventor: KUNSTADT G H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5131029	A	19920714	US 90571509	A	19900823	199231	B

Priority Applications (No Type Date): US 90571509 A 19900823
Patent Details:
Patent No Kind Lan Pg   Main IPC   Filing Notes
US 5131029   A   5 H04M-001/64

Abstract (Basic): US 5131029 A
The cellular telephone dialing **controller** comprises an operator switch, a **state machine** , digitally stored audio prompts and a Dual Tone multi-Frequency signal generator. At each dialing step the operator hears sequentially the numerals zero, one, etc. and the operator ''dials'' by closing the operator's switch when the proper number is played.
At completion of ''dialing'' the entire phone number is audibly replayed for operator approval, after which the call is automatically initiated, including the generation of Dual Tone Multi-Frequency as well as Off-Hook/On-Hook control signals.
USE/ADVANTAGE - For motor vehicle. The entire dialling operation is completed without visual participation or use of the operator's hands, to ensure driving **safety** .
Dwg. 1/1
Title Terms: CELLULAR; CAR; TELEPHONE; DIAL; CONTROL; NUMBER; SEQUENCE; HEARING; USER; DIAL; STEP; OPERATE; SWITCH; CLOSE; DIAL; NUMBER; CORRECT; NUMBER; HEARING
Derwent Class: W01
International Patent Class (Main): H04M-001/64
File Segment: EPI

35/5/8 **(Item 7 from file: 350)**
DIALOG(R)File 350:Derwent WPIX
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0015172 **Image available**
WPI Acc No: 1991-209793/199129
XRPX Acc No: N91-160156
Optical fibre link control safety **system - comprises loss of light detector producing at least two independent signals under fault condition and regulating laser output**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC)
Inventor: HEILING G M; KNODEL D A; PETERSON M J; SCHUELKE B A; SILJENBERG D W; SODERSTROM R L; TRNKA J T; KNADEL D A; PETESSON M J; SILKENBERG D W
Number of Countries: 017 Number of Patents: 011
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
EP 437162 A 19910717 EP 90480199 A 19901127 199129 B
AU 9067875 A 19910711 199135
CA 2032209 A 19910710 199138
BR 9100035 A 19911022 199147
CN 1054692 A 19910918 CN 90109824 A 19901214 199225
US 5136410 A 19920804 US 90462367 A 19900109 199234
AU 635798 B 19930401 AU 9067875 A 19901207 199320
EP 437162 A3 19920513 EP 90480199 A 19901127 199330
TW 215133 A 19931021 TW 90109593 A 19901114 199402
CA 2032209 C 19940118 CA 2032209 A 19901213 199409
KR 9407470 B1 19940818 KR 9020444 A 19901213 199622

Priority Applications (No Type Date): US 90462367 A 19900109
Cited Patents: NoSR.Pub; 1.Jnl.Ref; DE 3147555; EP 382243; GB 2195508; JP 62220633
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
EP 437162 A
Designated States (Regional): BE CH DE ES FR GB IT LI NL SE
EP 437162 A 16 H04B-010/12
AU 635798 B H04B-010/08 Previous Publ. patent AU 9067875
CN 1054692 A H04B-010/08
TW 215133 A G08B-025/01
CA 2032209 C H04B-010/12

(Basic): EP 437162 A

The interlock system comprises a device for detecting the loss of light on a fibre optic link. A **controller** , coupled to the detector, determines the **safety** condition of the link based on the output of the detector. The **controller** also controls the radiant energy output of an optical transmitter, based upon the determined **safety** condition, via redundant output control signals. A device coupled to the **controller** and responsive to the redundant control signals interconnects the output of the **controller** to transmitter drive circuitry to thereby adjust the radial energy output of the transmitter.

The **controller** pref. includes an electronic implementation of two independent **state machines** , each of which redundantly determines the connection state of the optical link between two optical link cards.

USE/ADVANTAGE - Medical technology, communications and computing. Reduces laser energy output to **safe** level when failure is detected.

36/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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07362467 **Image available**
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUB. NO.: 2002-230964 [JP 2002230964 A]
PUBLISHED: August 16, 2002 (20020816)
INVENTOR(s): MATSUDA TAKESHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD
APPL. NO.: 2001-019314 [JP 200119314]
FILED: January 29, 2001 (20010129)
INTL CLASS: G11C-007/00; G11C-011/413; G11C-011/417

ABSTRACT

PROBLEM TO BE SOLVED: To make the hold-time of write-in data **securable** without using a delay buffer in a semiconductor integrated circuit device in which a write-in control circuit for **securing** a hold-time at the time of a write-in cycle is built in.

SOLUTION: A write-cycle detector 102 detects a write-cycle by input of a system clock (a), a chip enable-signal (b), a write-enable signal (c), thereby a **state machine** 103 transits a state, a write-in control signal generator 104 generates a write-in control signal (g) negating with timing being earlier than negate-timing of the write-enable signal (c) synchronizing with the system clock (a) at the time of a specific state of a state (f). The hold-time of write-in data (h) for this write-in timing can be **secured** by writing write-in data (h) in a register 105 with the negate-timing of this write-in control signal (g).

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36/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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06787390 **Image available**
NON-VOLATILE SEMICONDUCTOR STORAGE

PUB. NO.: 2001-014871 [JP 2001014871 A]
PUBLISHED: January 19, 2001 (20010119)
INVENTOR(s): KASAI HISAMICHI
NISHIMURA NOZOMI
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 11-183228 [JP 99183228]
FILED: June 29, 1999 (19990629)
INTL CLASS: G11C-016/02; G06F-012/14

ABSTRACT

PROBLEM TO BE SOLVED: To prevent fabrication and leak of hold data even when a releasing method of a **security** function is discovered by erasing hold data of a memory means independently of setting of rewriting prohibition information when a read-out prohibition state is released by setting read-out prohibition information.

SOLUTION: When releasing a **security** function (**security** off) is instructed to a command interface 13, a **state machine** (erasing means) 14 of a flash memory checks cells 12a to 12c for protection in a protection information/ **security** information storing circuit 12, and judges whether it is in a rewriting prohibition state (protection on) of protection information or not. When it is in a rewriting prohibition state, setting protection information is neglected, hold data of all blocks 11a to 11c in a flash memory main body (memory means) is forcedly erased.

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36/5/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
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05061125 **Image available**
SPECIFICATION EXECUTION VERIFYING DEVICE

PUB. NO.: 08-016625 [JP 8016625 A]
PUBLISHED: January 19, 1996 (19960119)
INVENTOR(s): NAKAJIMA TAKESHI
TAMURA NAOKI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-144884 [JP 94144884]
FILED: June 27, 1994 (19940627)
INTL CLASS: [6] G06F-017/50
JAPIO CLASS: 45.4 (INFORMATION PROCESSING -- Computer Applications)

ABSTRACT

PURPOSE: To attain plural execution environments while performing the unitary management of the specifications as an abstract machine by carrying out the specifications based on the specification description produced at a specification defining part and the execution environment produced at an execution environment production part respectively.

CONSTITUTION: A specification defining part 103 defines an abstracted **state machine** as an abstract machine and uses this machine to produce the specification description. An execution environment production part 104 defines the abstracted **state machine** as a concrete machine based on the abstract machine define at the part 103 and produces an execution environment by means of the concrete machine. An execution part 105 carries out the specifications based on the specification description produced at the part 103 and the execution environment produced at the part 104. Thus a high abstract level is **secured** for description of the **state machine**, and it is not needed to apply the relating already given to the abstract machine to the concrete machine. Therefore the maintenance management is facilitated for the specifications.

36/5/8 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015812150 **Image available**
WPI Acc No: 2003-874354/200381
XRPX Acc No: N03-698068

BIOS device for computers, has internal memory to contain basic input/output system code and state machine to permit access to portion of code in response to authentication of portable token in communication with machine

Patent Assignee: INTEL CORP (ITLC)
Author: ARIS D L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6633981	B1	20031014	US 99336009	A	19990618	200381	B

Priority Applications (No Type Date): US 99336009 A 19990618
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6633981	B1		12	G06F-001/24	

Abstract (Basic): US 6633981 B1

NOVELTY - The device (135) has an internal memory to contain a basic input/output system (BIOS) code. A **state machine** controls and permits access to a portion of the BIOS code in response to **authentication** of a portable token (145) in communication with the machine. A random number generator produces signals corresponding to a

number for storage in the memory (110).

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) a method for controlling access through user **authentication**

(2) a program loaded in internal memory of a BIOS device.

USE - Used for controlling access to the electronic system e.g. computers, to maintain data **security** .

ADVANTAGE - The device is independent of the operations of the operating system for controlling access to stored information, thereby resulting in a robust **authentication** technique.

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of an electronic system.

Processor (105)

Main memory (110)

Bus (130)

BIOS device (135)

Token reader (145)

pp; 12 DwgNo 1/9

[illegible]: DEVICE; COMPUTER; INTERNAL; MEMORY; CONTAIN; BASIC; INPUT; [illegible]; SYSTEM; CODE; STATE; MACHINE; PERMIT; ACCESS; PORTION; CODE; [illegible]; AUTHENTICITY; PORTABLE; TOKEN; COMMUNICATE; MACHINE

[illegible] Class: T01

International Patent Class (Main): G06F-001/24

File Segment: EPI

36/5/9 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015687515 **Image available**

WPI Acc No: 2003-749704/200371

XRPX Acc No: N03-600939

Digital services unauthorized access control system in satellite video distribution system, comprises custom logic block with fixed algorithm to control access of non-volatile memory in conditional access module

Patent Assignee: HUGHES ELECTRONICS CORP (HUGA)

Inventor: COCCHI R P; CURREN C P; KAHN R M

Number of Countries: 031 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1345438	A2	20030917	EP 20034321	A	20030227	200371	B

Priority Applications (No Type Date): US 200285920 A 20020228

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1345438	A2	E	17	H04N-007/16	

Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

Abstract (Basic): EP 1345438 A2

NOVELTY - A conditional access module (CAM) connected to integrated receiver/decoder (126) has nonvolatile memory storing state information to provide desired functionality and **security** policies for accessing digital services. The nonvolatile memory and microprocessor non-volatile memory share a programming charge pump. A fixed state custom logic block is configured to control access of non-volatile memory.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) a method for limiting unauthorized access to digital services; and

(2) a conditional access module.

USE - For controlling unauthorized access of digital services, television programs, and pay-per-view (PPV) program services in satellite video distribution system.

ADVANTAGE - Since custom logic block performs a fixed algorithm, unauthorized access of digital services are limited, thereby protecting

unauthorized access of the non-volatile memory. Improves protection of memory content significantly, through isolation of memory from system bus module, system bus and microprocessor. Reduces manipulation of memory content and improves integrity of memory using fixed operation of a **state machine** provided by custom logic block.

DESCRIPTION OF DRAWING(S) - The figure shows an explanatory drawing of video distribution system.

control center (102)
up link center (104)
transmitter (105)
antenna (106)
satellite (108)
subscriber receiver station (110)
communication links (114,116)
integrated receiver/decoder (126)

pp; 17 DwgNo 1/7

Title Terms: DIGITAL; SERVICE; UNAUTHORISED; ACCESS; CONTROL; SYSTEM; SATELLITE; VIDEO; DISTRIBUTE; SYSTEM; COMPRISE; CUSTOM; LOGIC; BLOCK; FIX ; ALGORITHM; CONTROL; ACCESS; NON; VOLATILE; MEMORY; CONDITION; ACCESS; MODULE

Derwent Class: T01; U14; W02; W03

International Patent Class (Main): H04N-007/16

File Segment: EPI

36/5/11 **(Item 8 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

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Image available

WPI Acc No: 2003-576322/200354

XRPX Acc No: N03-458116

Stealth firewall for computer network, has state machine **which is preconfigured to make transition from restricting state to access state which causes packet filter to permit access to network**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)

Inventor: MARTIN B K

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030051155	A1	20030313	US 2001944996	A	20010831	200354	B

Priority Applications (No Type Date): US 2001944996 A 20010831

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030051155	A1		10	G06F-011/30	

Abstract (Basic): US 20030051155 A1

NOVELTY - A packet filter restricts access to internal network, and a **state machine** (250) is preconfigured to make a transition from restricting state to access state which causes the packet filter to permit access to the internal network based on the code in the received access requests.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) method for permitting access to network; and

(2) recorded medium storing program for permitting access to network.

USE - For computer networks e.g.internet.

ADVANTAGE - The access to the network protected by the stealth wall is **authenticated** by using a single **authentication** packet. Since the network is accessed by the requesting network device when the received access request consists of specified code, the network **security** is improved.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic view of the stealth firewall.

stealth firewall (210)
internet (220)

router (240)
state machine (250)
access code (260)
internal network (270)
pp; 10 DwgNo 2/3
Title Terms: FIREWALL; COMPUTER; NETWORK; STATE; MACHINE; TRANSITION; RESTRICT; STATE; ACCESS; STATE; CAUSE; PACKET; FILTER; PERMIT; ACCESS; NETWORK
Derwent Class: T01; U21; W01
International Patent Class (Main): G06F-011/30
File Segment: EPI

36/5/14 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

015149380 **Image available**
WPI Acc No: 2003-209907/200320
XRPX Acc No: N03-167400
Network recognition system for network security , comprises processor with several processing elements to analyze and evaluate portion of protocol using preset rules and policies
Patent Assignee: DILLARD J W (DILL-I); MCKINLEY W G (MCKI-I)
Inventor: DILLARD J W; MCKINLEY W G
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020191549	A1	20021219	US 2001298727	P	20010614	200320 B
			US 2002171917	A	20020614	

Priority Applications (No Type Date): US 2001298727 P 20010614; US 2002171917 A 20020614
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020191549	A1		20	H04L-012/28	Provisional application US 2001298727

Abstract (Basic): US 20020191549 A1
NOVELTY - A processor (20) has several processing elements (26,28,30,32) which analyze and evaluate a portion of the protocol stored in a buffer (18) using the preset rules and policies to determine an action. A **state machine** (34) tracks the order of transmission of the protocols between the networks (12,14) and initiates the determined action on the protocol. An output interface (24) transmits the protocol between the networks.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) Network processor; and
(2) Network protocol processing method.
USE - Network recognition system e.g. for asynchronous transfer mode (ATM), Ethernet, SONET, OC-48 and OC-12 based networks for network **security** and data communication.
ADVANTAGE - By using several processing elements connected in parallel, the processing speed is increased. By the use of preset rules/policies to determine an action, the efficiency of the system is improved.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the network recognition system.
Networks (12,14)
Buffer (18)
Processor (20)
Output interface (24)
Processing elements (26,28,30,32)
State machine (34)
pp; 20 DwgNo 1/14
Title Terms: NETWORK; RECOGNISE; SYSTEM; NETWORK; **SECURE** ; COMPRISE; PROCESSOR; PROCESS; ELEMENT; ANALYSE; EVALUATE; PORTION; PROTOCOL; PRESET ; RULE

Derwent Class: T01; W01
International Patent Class (Main): H04L-012/28
File Segment: EPI

36/5/24 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004 Thomson Derwent. All rts. reserv.

009206672 **Image available**
WPI Acc No: 1992-334093/199241
XRPX Acc No: N92-255015
User state machine for controlling memory network - interfaces to user and allows access for write or erase instructions only under predetermined conditions
Patent Assignee: INTEL CORP (ITLC)
Inventor: FANDRICH M L; KREIFELS J A; KYNETT V N; LEE K W; ROBINSON K B; KREIFFELS J A
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2672709	A1	19920814	FR 921500	A	19920211	199241	B
US 5463757	A	19951031	US 91655643	A	19910211	199549	
			US 94185449	A	19940121		
JP 3442088	B2	20030902	JP 9257311	A	19920212	200358	

Priority Applications (No Type Date): US 91655643 A 19910211; US 94185449 A 19940121
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2672709	A1		30	G06F-013/14	
US 5463757	A		15	G06F-012/00	Cont of application US 91655643
JP 3442088	B2		16	G11C-016/02	Previous Publ. patent JP 6028877

Abstract (Basic): FR 2672709 A
The user **State Machine** is designed to control a network of memory in a data processing system. The control includes circuits for writing to memory locations and for erasing memory locations. Logic circuits provide signals to read areas of the memory network and in response to instructions from the user to write or erase memory locations.
Additional logic circuits take data from the memory to prevent alteration of memory contents under predefined conditions.
ADVANTAGE - **Secure** control of write/erase operations on memory systems.
Dwg.2/6
Title Terms: USER; STATE; MACHINE; CONTROL; MEMORY; NETWORK; INTERFACE; USER; ALLOW; ACCESS; WRITING; ERASE; INSTRUCTION; PREDETERMINED; CONDITION
Derwent Class: T01
International Patent Class (Main): G06F-012/00; G06F-013/14; G11C-016/02
International Patent Class (Additional): G06F-012/14
File Segment: EPI

36/5/27 (Item 24 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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009[illegible]96 **Image available**
WPI Acc No: 1990-268999/199036
XRPX Acc No: N90-208219
Digital, high-speed movement control unit e.g. for aircraft - uses several servo-control microprocessors provided with trajectory path data via common system bus
Patent Assignee: HUGHES AIRCRAFT CO (HUGA)
Inventor: EVANS D D; GABALDON J B
Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4005042	A	19900830	DE 4005042	A	19900216	199036	B
US 4977494	A	19901211	US 89312105	A	19890217	199101	
DE 4005042	C2	19940519	DE 4005042	A	19900216	199418	

Priority Applications (No Type Date): US 89312105 A 19890217

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4005042	C2		16	G05B-019/403	

Abstract (Basic): DE 4005042 A

The systems bus (13) carries multi-dimensional bus data interfaces with a majority of local micro-processors (24), one for each dimension, via a majority of dual access storage structures (RAMs) (21), one for each local micro-processor. A local decision device controls access to each dual access storage structure (RAM). This simplifies the elimination of standby conditions during data transmission between the system bus and the storage (21) and between the local micro-processor and the storage.

The decision device employs the methods of a status engine of a programmable, logical component. This engine implements an operational [illegible], in which transmission switching between a local microprocessor [illegible] dual access storage allows an interruption and completes the transmission without standby conditions. The status engines and the [illegible] access storage are controlled via a signal pulse, which is twice as fast as the selection response of the local microprocessor. This is involved in the implementation of the status engines, in order to **secure** storage access for the systems bus and the local microprocessor, which has priority in this operation.

ADVANTAGE - Improved processing time and control algorithm checks.

File 348:EUROPEAN PATENTS 1978-2004/Mar W04
(c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040401,UT=20040325
(c) 2004 WIPO/Univentio

Set	Items	Description
S1	10985	(STATE OR STATEFUL)()MACHINE? ? OR FINITE()STATE? ?
S2	35772	(CURRENT OR RECENT OR EXISTING OR PRESENT)(1W)(STATE? ? OR CONDITION? ?)
S3	9698	(PAST OR PREVIOUS OR PRIOR OR PRECEDING OR LAST OR EARLIER OR FORMER)(1W)(STATE? ? OR CONDITION? ?)
S4	[illegible]327	(FUTURE OR ALLOWED OR ALLOWABLE OR PERMITTED OR PERMISSIBLE OR AUTHORIZED OR AUTHORISED OR ACCEPTED OR ACCEPTABLE OR NORMAL OR EXPECTED OR RANGE? ?)(5N)(STATE? ? OR CONDITION? ?)
S5	4348	DIGITAL()SIGNATURE? ?
S6	6921	(PUBLIC OR PRIVATE)()KEY? ?
S7	43010	CRYPTO? OR CRYPTANALY? OR CIPHER? OR CYPHER? OR ENCRYPT? OR ENCIPHER? OR SCRAMBL? OR DECRYPT? OR DECIPHER? OR UNENCRYPT? OR UNSCRAMBL?
S8	30	S1(50N)S2:S4(50N)S5:S7
S9	369449	AUTHENTICAT? OR SECUR?
S10	37	S1(50N)S2:S4(50N)S9
S11	31	S10 NOT S8
S12	2080	FINITE()STATE()(MACHINE? ? OR DEVICE? ? OR UNIT? ? OR AUTOMATA)
S13	156	S1(50N)S2(50N)S3:S4
S14	33	S1(50N)S3(50N)S4
S15	28	S12(50N)S2(50N)S3:S4
S16	1	S12(50N)S3(50N)S4
S17	28	S15:S16
S18	26	S17 NOT (S8 OR S11)
S19	7	S1(50N)S5
S20	29	S1(50N)S6
S21	215	S1(50N)S7
S22	252	S1(50N)S9
S23	35	S19:S20
S24	31	S23 NOT (S8 OR S11 OR S18)
S25	18	S12(50N)S7(50N)S9
S26	11	S25 NOT (S8 OR S11 OR S18 OR S24)
S27	[illegible]	S12(30N)S2:S4(30N)CONTROLLER? ?
S28	[illegible]56	S12(30N)S2
S29	19	S12(30N)S3
S30	78	S12(30N)S4
S31	202	S28:S30
S32	35	S31/TI,AB,CM
S33	27	S32 NOT (S8 OR S11 OR S18 OR S24 OR S26:S27)

18/9/6 (Item 6 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00695140
Improved finite state machine for process control
Verbesserter endlicher Zustandsautomat fur eine Prozesssteuerung
Machine a nombre fini d'etat ameliore pour une commande processus
PATENT ASSIGNEE:
AT&T Corp., (589370), 32 Avenue of the Americas, New York, NY 10013-2412, (US), (Proprietor designated states: all)
INVENTOR:
Flora-Holmquist, Alan R., 413 Republic, Batavia, Illinois 60510, (US)
Mills, Thomas L., 2781 Greenfield Drive, Lisle, Illinois 60532, (US)
O'Grady, James Day, 354 Sunset Avenue, Aurora, Illinois 60506, (US)
LEGAL REPRESENTATIVE:
Watts, Christopher Malcolm Kelway, Dr. (37391), Lucent Technologies (UK) Ltd, 5 Mornington Road, Woodford Green Essex, IG8 0TU, (GB)
PATENT (CC, No, Kind, Date): EP 662651 A2 950712 (Basic)
EP 662651 A3 960828
EP 662651 B1 010919
APPLICATION (CC, No, Date): EP 94309194 941209;
PRIORITY (CC, No, Date): US 174641 931228; US 174646 931228; US 174642 931228
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G05B-019/042
CITED REFERENCES (EP B):
PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON INDUSTRIAL ELECTRONI CONTROL, AND INSTRUMENTATION. (IECON), CAMBRIDGE, MASSACHUSETTS, NOV. 3 - 6, 1987, vol. VOL. 1 OF 2, no. 1987, 3 November 1987, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 477-481, XP000041863 LAURIE R. M. ET AL: "A STATE MACHINE ARCHITECTURE OPTIMIZED FOR SEQUENTIAL CONTROL"
ADVANCES IN INSTRUMENTATION AND CONTROL, vol. 48, no. PART 02, 1 January 1993, pages 985-997, XP000435402 SMITH M.: "THE FUNDAMENTAL THEORY OF STATE LOGIC CONTROL";

ABSTRACT EP 662651 A3
A model of a finite state machine suited for implementation in a microcomputer includes logical specifications stored in memory which determine whether a change of outputs should be effected in response to predetermined combinations of input parameters and whether a change of state should be effected based on stored logical conditions of input parameters. Additional control of the flow of the steps of the finite state machine are under the control of the designer wherein a designer controlled variable permits a selection following a state transition as to whether or not an immediate test or input parameters will be made to determine whether additional actions are required or whether a return to a determination of state transition is to be made. (see image in original document)
ABSTRACT WORD COUNT: 143
NOTE:
Figure number on first page: 8

LEGAL STATUS (Type, Pub Date, Kind, Text):
Grant: 010919 B1 Granted patent
Application: 950712 A2 Published application (Alwith Search Report ;A2without Search Report)
Oppn None: 020911 B1 No opposition filed: 20020620
Search Report: 960828 A3 Separate publication of the European or International search report
Examination: 970416 A2 Date of filing of request for examination: 970212
Examination: 970917 A2 Date of despatch of first examination report: 970801
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count

CLAIMS A	(English)	EPAB95	2028
CLAIMS B	(English)	200138	752
CLAIMS B	(German)	200138	690
CLAIMS B	(French)	200138	847
SPEC A	(English)	EPAB95	7376
SPEC B	(English)	200138	6471
Total word count - document A			9406
Total word count - document B			8760
Total word count - documents A + B			18166

SPECIFICATION EP 662651 A2

Background of the Invention

This invention relates generally to computer implemented finite state machines which are suited for process control applications. This invention is more specifically directed to an implementation of a finite state machine in which the sequence of execution of steps can be controlled by a user for each state of the machine.

As used herein, a finite state machine refers to a sequential system in which input parameters determine the state of operation of the machine. An implementation of a finite state machine is described in U.S. Patent No. 5,301,100 entitled "Method of an Apparatus for Constructing a Control System and Control System Created Thereby". This application describes a logic table for implementing the finite state machine in which a specific organization of data represents application logic conditions expressed utilizing logical AND and OR operators. FIGs. 1-7 in the present application describe aspects of such a prior art finite state machine implementation. FIG. 4 of the present application illustrates a finite state machine model as contemplated by this prior art.

In the finite state machine model in accordance with the above-referenced prior art, a change of input parameters is required following a change of state transition before a test is made to determine if output actions are required in response to predetermined input parameter conditions. In certain applications it is desirable to be able to process such input conditions although a change in input parameters may not be required since a change of state. One way of inducing such input processing is to utilize an additional input parameter not related to the processed input parameters which can be toggled solely to cause a re-evaluation of input parameters. Such an input functions as a "kicker" to initiate an evaluation of input actions. The use of such an input kicker is undesirable in that it adds to the number of inputs and must be initiated at an appropriate time relative to the state of the finite state machine in order to be effective. Thus, there exists a need for an improved finite state machine model which overcomes this deficiency.

The above referenced prior art implementation of a finite state machine is encoded in a fixed size data structure in which logical vectors are stored in memory to define changes in output actions and change of state transitions in the finite state machine. The fixed coding arrangement requires that the maximum number of logical vectors utilized for a given set of conditions be utilized for the other sets of like conditions. This results in individual vectors which are blank, i.e. contain no logical data, since each fixed memory allocation must reflect the maximum possible number of vectors. Thus, there exists a need for an improved implementation of a finite state machine which minimizes memory usage.

In the finite state machine model in accordance with the above-referenced prior art, a plurality of "AND" vectors are stored in an application logic table and define the processing steps implemented by the general flow of the state machine. Input parameters are represented by an input vector having a given bit length. The AND vectors are each of the same length as the input vector and are compared with the input vector on a bit-by-bit basis to make logical determinations in accordance with the state machine.

For a number of applications, the AND vectors of the prior art may in fact consist of a single set bit. Thus, the combination of all bits in such an AND vector with the input vector are unnecessary in that such comparisons can not yield a TRUE result. The comparison with AND vectors with the input vector on a bit-by-bit basis requires a number of execution cycles. Thus, there exists a need to enhance the execution speed by minimizing unnecessary bit-by-bit comparisons.

Summary of the Invention

It is an object of the present invention to provide an improved finite state machine in which the sequence of execution of steps can be selectively controlled dependent on the state of the machine. It is a further object of the present invention to provide an improved finite state machine implementation which permits input parameters to be selectably evaluated following a state transition based on preprogrammed control.

It is a further object of the present invention to provide an improved finite state machine suited for implementation as vectors stored in memory of a microprocessing system in which nonfixed size data structures are permitted.

It is another object of the present invention to provide an improved finite state machine implementation which permits certain AND vectors to be compared with an input vector without requiring a bit-by-bit comparison.

In accordance of an embodiment of the present invention, a process control apparatus includes a microcomputer which implements a finite state machine having a plurality of possible states. An input register receives input signals in which signal represents a condition associated with a process monitored by the finite state machine. An output register generates output signals representing commands that control a function associated with the controlled process. An application table stores a set of vectors in memory for each state of the finite state machine. The input signals are compared with the set of vectors in order to make a decision on whether a transition to a different state is to be made. Following the change of state, a determination is made of whether a stored set of conditions associated with the changed state should be compared with the input signals. This determination is based on whether a predetermined proceed flag stored for each state of the machine is setThe comparison is made if the proceed flag is set; if the proceed flag is not set, the comparison is not made and control passes to a next step.

In accordance with an embodiment of the present invention, a finite state machine has a plurality of states and corresponding sets of selection vectors in which logical data is selectively stored to define logical conditions. An address locator corresponding to a set of the selection vectors is stored in memory for each state of the finite state machine. A section of memory associated with the microcomputer stores the set of selection vectors consisting of groups of vectors defining logical conditions. A count of the number of logical conditions within each group is stored as part of the group in order to permit different numbers of vectors to be stored in each group. The count of vectors within a group is utilized during execution of the finite state machine to determine the number of vector conditions to be read and tested relative to another vector.

In a preferred embodiment a predetermined null value is assigned to an address locator to represent that a corresponding set of selection words does not exist. The null value is interpreted as requiring no further action; the process proceeds to the next step as defined in accordance with the finite state machine.

In accordance with an embodiment of the present invention, an application table stores sets of conditions in memory as AND vectors which are compared against the input vector defined by the input register. AND vectors having a single set bit are identified and translated into a corresponding AND index vector in which the bit position having the set bit is encoded. The AND index also includes an index flag identifying the vector as an AND index vector as opposed to a normal full length AND vector. The AND index vector replaces the corresponding AND vector from which it was derived. During the execution of the finite state machine, a determination is made if a vector is an AND index vector based on the index flag. If a vector is determined to be an AND index vector, the stored bit position contained in the AND index vector is decoded and utilized to identify a corresponding bit position in the input vector, and a TRUE/FALSE determination is made of the identified bit in the input vector. This completes the equivalent comparison of the index vector with the input vector. Thus, it will be apparent that a bit-by-bit comparison is eliminated and thereby execution speed is increased.

27/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01654749
Common data path rake receiver for a CDMA demodulator circuit
Gemeinsamer Datenpfad Rake Empfanger fur CDMA Demodulator
Recepteur du type Rake pour un demodulateur a AMRC avec chemin de donnees commun
PATENT ASSIGNEE:
STMicroelectronics, Inc., (723062), 1310 Electronics Drive, Carrollton, TX 75006-5039, (US), (Applicant designated States: all)
INVENTOR:
Cervini, Stefano, 8548 Via Mallorca Dr., No. E, La Jolla, California 92037, (US)
LEGAL REPRESENTATIVE:
Style, Kelda Camilla Karen et al (75491), Page White & Farrer, 54 Doughty Street, London WC1N 2LS, (GB)
PATENT (CC, No, Kind, Date): EP 1361670 A1 031112 (Basic)
APPLICATION (CC, No, Date): EP 2003252826 030506;
PRIORITY (CC, No, Date): US 141460 020507
DESIGNATED STATES: AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES; FI; FR; GB; GR; HU; IE; IT; LI; LU; MC; NL; PT; RO; SE; SI; SK; TR
EXTENDED DESIGNATED STATES: AL; LT; LV; MK
INTERNATIONAL PATENT CLASS: H04B-001/707
ABSTRACT WORD COUNT: 93
NOTE:
Figure number on first page: NONE

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200346	1407
SPEC A	(English)	200346	6936
Total word count - document A			8343
Total word count - document B			0
Total word count - documents A + B			8343

27/3,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00693721
Method of controlling multiple processes using finite state machines.
Verfahren zur Steuerung mehrerer Prozesse mit Endlichkeitszustandsgeraten.
Methode de controle de procedes multiples des machines dans un etat defini.
PATENT ASSIGNEE:
AT&T Corp., (589370), 32 Avenue of the Americas, New York, NY 10013-2412, (US), (applicant designated states: DE;ES;FR;GB)
INVENTOR:
Schell, William M., 910 Johnston Drive, Watchung, New Jersey 07060, (US)
Story, Guy Ashley, 151 Spring Street, New York, New York 10012, (US)
LEGAL REPRESENTATIVE:
Watts, Christopher Malcolm Kelway, Dr. et al (37391), AT&T (UK) Ltd. 5, Mornington Road, Woodford Green Essex, IG8 0TU, (GB)
PATENT (CC, No, Kind, Date): EP 661882 A1 950705 (Basic)
APPLICATION (CC, No, Date): EP 94309174 941209;
PRIORITY (CC, No, Date): US 175059 931229
DESIGNATED STATES: DE; ES; FR; GB
INTERNATIONAL PATENT CLASS: H04N-007/173;
ABSTRACT WORD COUNT: 149

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB95	529
SPEC A	(English)	EPAB95	6859

Total word count - document A 7388
Total word count - document B 0
Total word count - documents A + B 7388

...SPECIFICATION processes needed to provide interactive television services to multiple users simultaneously. This problem is solved in accordance with the present invention by using hierarchies of **finite state machines** (FSMs).

Many control devices have multiple **states** with **permitted** transitions between **states** . Such devices can **range** from simple **controllers** containing a few relays, logic circuits or a single microprocessor to complex control systems including multiple processors. Such control devices can often be analyzed by simulating them as a series of **finite state machines** , also called finite automata. FSMs themselves can be implemented by computer programs. Thus, it is feasible to design and implement a control system as a...

27/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00616092
CALL DISTRIBUTOR
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DISTRIBUTEUR D'APPELS
PATENTEE:
Applied Technology, Inc., (1750631), 800 North Main Street, Glen Ellyn, IL 60137, (US), (applicant designated states: DE;FR;GB;IE;NL)
INVENTOR:
BRADY, Patrick, 2 S. 671 Arrowhead Drive, Wheaton, IL 60187, (US)
LEGAL REPRESENTATIVE:
Barnfather, Karl Jon, Dr. et al (79232), Withers & Rogers, Goldings House, 2 Hays Lane, London SE1 2HW, (GB)
PATENT (CC, No, Kind, Date): EP 647381 A1 950412 (Basic)
EP 647381 A1 951025
EP 647381 B1 990519
WO 9400945 940106
APPLICATION (CC, No, Date): EP 93916803 930625; WO 93US6129 930625
PRIORITY (CC, No, Date): US 904196 920625
DESIGNATED STATES: DE; FR; GB; IE; NL
INTERNATIONAL PATENT CLASS: H04M-003/42; H04M-003/50;
NOTE:
No A-document published by EPO
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	9920	498
CLAIMS B	(German)	9920	438
CLAIMS B	(French)	9920	602
SPEC B	(English)	9920	10605

Total word count - document A 0
Total word count - document B 12143
Total word count - documents A + B 12143

...INFORMATION the top of the queue for reception by the LCP process 116.

In the embodiment under consideration, the LCP process 116 itself is a simple **finite state machine** that responds to messages appearing on the top of the digital signal processor message queue 114 in the context of its **current state** . For example, in one embodiment of the invention the telephony interface **controller** module 102 has two states: Idle and Answer. The receipt of an ONHOOK message during the Idle state is ignored, while the receipt of an...

27/3,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00324615
Bus controller command block processing system.
Steuerungsblockverarbeitungssystem fur Bussteuerung.
Systeme de traitement de blocs de commande pour controleur de bus.
PATENT ASSIGNEE:
UNITED TECHNOLOGIES CORPORATION, (206570), United Technologies Building 1, Financial Plaza, Hartford, CT 06101, (US), (applicant designated states: DE;FR;GB)
INVENTOR:
Grant, John L., 612 North Walnut Street, Colorado Springs Colorado 80905, (US)
Stracher, Edward, 3136 Maverick Drive, Colorado Springs Colorado 80918, (US)
LEGAL REPRESENTATIVE:
Waxweiler, Jean et al (19251), OFFICE DENNEMEYER S.a.r.l. P.O. Box 1502, L-1015 Luxembourg, (LU)
PATENT (CC, No, Kind, Date): EP 327782 A1 890816 (Basic)
APPLICATION (CC, No, Date): EP 88630022 880208;
PRIORITY (CC, No, Date): EP 88630022 880208
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: G06F-013/28;
ABSTRACT WORD COUNT: 61

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF1	844
SPEC A	(English)	EPABF1	4590
Total word count - document A			5434
Total word count - document B			0
Total word count - documents A + B			5434

...SPECIFICATION single chip, but that it also reduces the load on the CPU.

Referring now to Figure 2, there is shown a block diagram of bus **controller** 100. On the left, encoder/decoder 102 converts parallel data to serial form and applies the conventional Manchester II coding scheme as required by the standard. Unit 102 is controlled in turn by bus control module 104, a simple **finite state machine** the sequence of which is shown in Figure 3. The **normal** waiting **state** is at the top of the figure waiting for a request from the command block processor 110 to perform a bus transfer. If the transfer...

27/3,K/5 **(Item 1 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00349845 **Image available**
MODE CONTROLLER FOR SIGNAL ACQUISITION AND TRACKING IN AN ULTRA WIDEBAND COMMUNICATION SYSTEM
MODULE DE COMMANDE DE MODE, DESTINE A L'ACQUISITION ET A LA POURSUITE DE SIGNAL DANS UN SYSTEME DE COMMUNICATION TRES LARGE BANDE
Patent Applicant/Assignee:
XTREMESPECTRUM INC, Suite 700, 8133 Leesburg Pike, Vienna, VA 22182, US, US (Residence), US (Nationality)
Inventor(s):
MILLER Timothy K, Apartment 114, 1444 Rhode Island Avenue N.W., Washington, DC 20005, US,
[illegible] Richard, 15700 Wayne Avenue, Laurel, MD 20707, US,
Legal Representative:
[illegible] Bradley D (agent), Oblon, Spivak, McClelland, Maier & Neustadt, P.C., Fourth Floor, 1755 Jefferson Davis Highway, Arlington, VA 22202, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200232066 A2-A3 20020418 (WO 0232066)

Application: WO 2001US27747 20011002 (PCT/WO US0127747)
Priority Application: US 2000685197 20001010
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU
CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP
KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU
SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) GH GM KE LS MW MZ SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 15351

Fulltext Availability:
Detailed Description

Detailed Description
... the same as the statistical properties of A + Cyn.. Then a reasonable approximation of the absolute value is
I Xj =A +0771 (7)
A mode **controller** of the present invention implements **finite state machines** .

Figure 4A is a state diagram of the mode **controller** of the **present** invention. **State** 141 is an acquire state machine for acquiring the incoming signal during acquisition mode. State 142 is a track state machine for tracking the incoming signal during the tracking/detection mode of operation. The value of L drives the mode **controller** by determining when the mode **controller** should transition between states and in which mode the receiver should operate. The mode controller starts in initial state 140. The signal is then acquired...

27/3,K/6 **(Item 2 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00773107 **Image available**
PROGRAMMABLE STEPPER MOTOR CONTROLLER AND METHOD THEREFOR
CONTROLEUR PROGRAMMABLE DE MOTEUR PAS A PAS ET PROCEDE
Patent Applicant/Assignee:
LEXMARK INTERNATIONAL INC, Intellectual Property Law Dept., 740 West New Circle Road, Lexington, KY 40550, US, US (Residence), US (Nationality)
Inventor(s):
RADEMACHER Timothy John, 1713 Shenandoah Drive, Lexington, KY 40504, US
MAYO Randall David, 103 Louisa Lane, Georgetown, KY 40324, US
Legal Representative:
LAMBERT D Brent, Lexmark International, Inc., Intellectual Property Law Dept., 740 West New Circle Road, Lexington, KY 40550, US
Patent and Priority Information (Country, Number, Date):
Patent: WO 200106635 A1 20010125 (WO 0106635)
Application: WO 2000US7889 20000324 (PCT/WO US0007889)
Priority Application: US 99352972 19990714
Designated States: AE AG AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE
DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC
LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK
SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
(OA) BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
(AP) GH GM KE LS MW SD SL SZ TZ UG ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 4445

Fulltext Availability:
Detailed Description

Claims

English Abstract
...system and method for controlling a stepper motor wherein the amount of memory space needed to store a phase table is minimized. The stepper motor **controller** (100) comprises a memory (110) sized to store data representing a plurality of states for current outputs to be supplied to a first winding of a stepper motor and from which are derived current outputs for the first winding and a second winding of the stepper motor. A **finite state machine** (120) is coupled to the memory. The **finite state machine** (120) comprises a first address register that stores an address for data in the memory for a **present state** of the first winding and a second register that stores an address for data in the memory for a **present state** of the second winding. When the **finite state machine** (120) receives as input a step control (150) or command signal, it reads a bit pattern (122) from the memory at an address corresponding to...

Detailed Description
... system and method for
controlling a stepper motor wherein the amount of memory space needed to store a phase table is minimized. The stepper motor **controller** comprises a memory sized to store data representing a plurality of states for current outputs to be supplied to a first winding of a stepper motor and from which are derived current outputs for the first winding and a second winding of the stepper motor. A **finite state machine** is coupled to the memory. The **finite state machine** comprises a first register that stores an address for data in the memory for a **present state** of the first winding and a second register that stores an address for data in the memory for a **present state** of the second winding. When the **finite state machine** receives as input a step control or command signal, it reads a bit pattern from the memory at an address corresponding to the contents of...

Claim
I . A stepper motor **controller** comprising:
a memory for storing data representing a plurality of states for current outputs to be supplied to a first winding of a stepper motor and from which are derived current outputs for the first winding and a second winding of the stepper motor; and
a **finite state machine** coupled to the memory, the **finite state machine**
comprising a first register that stores an address for data in the memory for a **present state** of the first winding and a second register that stores an address for data in the I 0 memory for a **present state** of the second winding, wherein the **finite state machine** receives as input a step command signal and in response thereto reads a bit pattern from the memory at an address corresponding to the contents...

27/3,K/7 **(Item 3 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00483550 **Image available**
MEMORY CONTROLLER IN A MULTI-PORT BRIDGE FOR A LOCAL AREA NETWORK
CONTROLEUR DE MEMOIRE DANS UNE PASSERELLE MULTI-PORTS DESTINEE A UN RESEAU LOCAL
Patent Applicant/Assignee:
SONY ELECTRONICS INC,
PHAM Son Minh,
Inventor(s):
PHAM Son Minh,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9914902 A1 19990325
Application: WO 98US18698 19980909 (PCT/WO US9818698)
Priority Application: US 9759171 19970917; US 9825355 19980218
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES

FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD
MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US
[illegible] YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE
[illegible] DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN
[illegible] ML MR NE SN TD TG
[illegible] Language: English
[illegible] Word Count: 19821
[illegible] Availability:
Claims

English Abstract
...providing an interface between the switch engine and an external processor. The switch engine includes the memory controller, a bus controller and a look-up **controller** , each preferably including a finite state machine. The memory **controller** provides an interface between the memory and the communication bus by including a command decoder for [illegible] bus commands received from the communication bus. For example, [illegible] command decoder provides a response to memory read and write bus commands. In addition, the memory **controller** includes a memory control **finite state machine** for controlling operation of the memory **controller** according to the bus commands received from the command decoder. The memory **controller** also includes logic and address registers for providing appropriate row and column addresses to the memory device according to a **current state** of the memory control **finite state machine** . Because the memory control **finite state machine** controls operation of the memory **controller** , memory read and write operations are performed with a minimum of delay, thereby increasing the throughput capacity of the multi-port bridge.

Claim
... a multi-port bridge for a local area network wherein the communication bus interconnects a plurality of ports of the multi-port bridge, the [illegible] by
controller comprising:
a. a command decoder coupled to the communication bus for receiving bus commands from the communication bus and for forming an operation control signal indicative of a type of bus command received;
b. a memory control **finite state machine** coupled to receive the operation
control signal from the command decoder, the memory control **finite state**
machine having a plurality of states;
I I C. means for forming a plurality of memory control signals according to a **current state** of the memory control **finite state machine** wherein the memory
control signals are coupled to control inputs of the memory device; and
d. means for forming row and column addresses according to memory address data received from the communication bus, the row and column addresses for coupling to address inputs of the memory device.

2 The memory **controller** according to claim I wherein the communication bus includes control signal lines and data lines and wherein the command decoder is coupled to the control...

27/3,K/8 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
[illegible] WIPO/Univentio. All rts. reserv.

[illegible] **Image available**
PREVENTING A SOURCE FROM BECOMING A DESTINATION PORT IN A MULTI-PORT BRIDGE
TECHNIQUE DE SELECTION DESTINEE A EVITER QU'UN PORT SOURCE NE DEVIENNE UN PORT DE DESTINATION DANS UNE PASSERELLE MULTI-PORTS DESTINEE A UN RESEAU LOCAL
Patent Applicant/Assignee:
SONY ELECTRONICS INC,
VASA Suresh L,
Inventor(s):
VASA Suresh L,

Patent and Priority Information (Country, Number, Date):
Patent: WO 9914892 A2 19990325
Application: WO 98US18769 19980909 (PCT/WO US9818769)
Priority Application: US 9759171 19970917; US 9864676 19980422
Designated States: AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM HR HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 12937

Fulltext Availability:
Detailed Description

Detailed Description
... 304 latches addresses from the communication bus 102 and provides them to the transceiver 308. The registers 304 also contain a counter for storing a **current state** of the **finite state machine** of the port and registers for storing parameters for use by the **finite state machines** of the port.

... also includes a memory pointer FIFO buffer 306 coupled between ... communication bus 102 and the port **controller** 300. The memory ... buffer 306 stores memory pointers (explained herein) for data ... being queued in the packet buffers 206 (Fig. 3) of the...

27/3,K/9 **(Item 5 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT
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00252793 **Image available**
CALL DISTRIBUTOR
DISTRIBUTEUR D'APPELS
Patent Applicant/Assignee:
TELEDATA SOLUTIONS INC,
Inventor(s):
BRADY Patrick,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9400945 A1 19940106
Application: WO 93US6129 19930625 (PCT/WO US9306129)
Priority Application: US 92904196 19920625
Designated States: AT AU BB BG BR CA CH CZ DE DK ES FI GB HU JP KP KR LK LU MG MN MW NL NO NZ PL PT RO RU SD SE SK UA AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 12324

... Availability:
... Description

... Description
... ... top of the queue for reception by the LCP process 116.

In the embodiment under consideration, the LCP process 116 itself is a simple **finite state machine** that responds to messages appearing on the top of the digital signal processor message queue 114 in the context of its **current state** . For example, in one embodiment of the invention the telephony interface **controller** module 102 has two states: Idle and Answer. The receipt of an ONHOOK message during the ... state is

33/5,K/8 (Item 8 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
(c) 2004 European Patent Office. All rts. reserv.

00893384
Method and system for testing software using a finite state machine
Verfahren und Anordnung zum Testen von Software unter Verwendung eines endlichen Automaten
Methode et systeme de test de logiciel utilisant une machine a nombre fini d'etats
PATENT ASSIGNEE:
SUN MICROSYSTEMS, INC., (1392735), 2550 Garcia Avenue, MS PAL1-521, Mountain View, California 94043-1100, (US),
INVENTOR:
Carter, Daniel H., 2 Boulder Crescent No. 8, Colorado Springs, Colorado 80903, (US)
LEGAL REPRESENTATIVE:
Hanna, Peter William Derek et al (72341), Tomkins & Co., 5 Dartmouth Road , Dublin 6, (IE)
PATENT (CC, No, Kind, Date): EP 817048 A1 980107 (Basic)
APPLICATION (CC, No, Date): EP 97201883 970619;
PRIORITY (CC, No, Date): US 674355 960701
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
INTERNATIONAL PATENT CLASS: G06F-011/00

ABSTRACT EP 817048 A1
A computer-implemented method and computer system for testing a target software product (22) are disclosed. The method includes constructing a finite state machine (20,60) in which portions of the target product are ascribed to states (34) of the state machine. The state machine may correspond to a predetermined test case for the target software product. A number of state functions are provided, each of the state functions performing at least one verification on the target software product. The state functions also may include means for transitioning from one state to the next, for example, by a "next window" a "previous window" action if the target software program is a windows-based program. The state functions may also verify that a current state in which the state machine exists is a correct state, may verify information that is supposed to have been written to a memory is written in fact to the memory, and may verify that the path to the information is correct. Information is furnished to the state machine for use by the target software product portions ascribed to states of the state machine. The information may include test case information from a test computer to the target software product as required by a test case being performed.
ABSTRACT WORD COUNT: 209
LEGAL STATUS (Type, Pub Date, Kind, Text):
Application: 980107 A1 Published application (A1with Search Report ;A2without Search Report)
Change: 980916 A1 Designated Contracting States (change)
Withdrawal: 990512 A1 Date on which the European patent application was deemed to be withdrawn: 980708
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:
Available Text Language Update Word Count
CLAIMS A (English) 9802 1971
DESC A (English) 9802 5724
Total word count - document A 7695
Total word count - document B 0
Total word count - documents A + B 7695

...CLAIMS 20, 60) comprises;
furnishing data required by at least one portion of said target software product ascribed to one of said states (34) of said **finite state machine** ; or
furnishing information to said state machine comprises furnishing a next window command to transition from a **current state** of said **finite state machine** to another state of said **finite state machine**

, and to cause said target computer product to display a next window to a user; or
furnishing an information input to receive user supplied information...

...comprises;
providing for furnishing data required by at least one portion of said target software product ascribed to one of said states (34) of said **finite state machine** ; or
providing for furnishing a next window command to transition from a **current state** of said **finite state machine** to another state of said **finite state machine** , and to cause said target computer product to display a next window (28) to a user; or
providing for furnishing an information input to receive...

33/5,K/9 (Item 9 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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0789724
Method for control of a process flow according to a specified behavior with a computer
Verfahren zur Steuerung eines Prozessablaufs nach von einem Rechner spezifizierten Verhalten
Methode pour le controle d'un deroulement de processus selon un comportement specifie par ordinateur
PATENT ASSIGNEE:
SIEMENS AKTIENGESELLSCHAFT, (200520), Wittelsbacherplatz 2, 80333 Munchen , (DE), (Proprietor designated states: all)
INVENTOR:
Brandin, Bertil, Dr., Baumstrasse 11, 80469 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 806735 A1 971112 (Basic)
EP 806735 B1 030326
APPLICATION (CC, No, Date): EP 96107107 960506;
PRIORITY (CC, No, Date): EP 96107107 960506
DESIGNATED STATES: AT; CH; DE; FR; GB; IT; LI
INTERNATIONAL PATENT CLASS: G06F-017/50
CITED PATENTS (EP B): EP 445942 A; EP 577298 A
CITED REFERENCES (EP B):
IEEE TRANSACTIONS ON AUTOMATIC CONTROL, vol. 39, no. 2, February 1994, NEW YORK US, pages 329-342, XP000605069 BRANDIN ET AL: "supervisory control of timed discrete-event systems"
COMPUTER AIDED VERIFICATION 7TH INTERNATIONAL CONFERENCE CAV 95 PROCEEDINGS, 3 July 1995, LIEGE BELGIUM, pages 279-292, XP000604449 AZIZ ET AL: "supervisory control of finite state machines";

ABSTRACT EP 806735 A1
A new approach to the modelling and control of timed state based [illegible] proposed. Instead of the treatment of time units the [illegible] treats activities directly thus achieving much smaller models [illegible] supervising process controllers. As well the amount of computations [illegible] analyse and generate the controller is highly reduced. A new computation method for time bounds is described. Such an approach and the corresponding technology is directly applicable to fields such as automated manufacturing, transport systems and communications systems, and offers important advantages over other existing approaches, mainly: automated coding of supervisory control strategies in industrial control systems and the very compact modelling of timed state based processes.
ABSTRACT WORD COUNT: 111
NOTE:
Figure number on first page: 7
LEGAL STATUS (Type, Pub Date, Kind, Text):

Grant:	030326	B1	Granted patent
Application:	971112	A1	Published application (A1with Search Report ;A2without Search Report)
Oppn None:	040317	B1	No opposition filed: 20031230
Examination:	980225	A1	Date of filing of request for examination: 971218

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	199711W1	1550
CLAIMS B	(English)	200313	1553
CLAIMS B	(German)	200313	1413
CLAIMS B	(French)	200313	1659
SPEC A	(English)	199711W1	5148
SPEC B	(English)	200313	5601
Total word count - document A			6700
Total word count - document B			10226
Total word count - documents A + B			16926

...CLAIMS an initial state of the process flow and continuing step by step for each respective further state of at least the first and the second **finite state machine** , it is analysed which state transitions are possible according to the description of the respective **finite state machine** and it is also checked which **state** transitions are **allowed** according to the specificationautomat, whereas only such state transitions are integrated in the processautomat which are possible and allowed;
d) the process flow is being...

...CLAIMS an initial state of the process flow and continuing step by step for each respective further state of at least the first and the second **finite state machine** , it is analysed which state transitions are possible according to the description of the respective **finite state machine** and it is also checked which **state** transitions are **allowed** according to the specificationautomat, whereas only such state transitions are integrated in the processautomat which are possible and allowed;
d) the process flow is being...

33/5,K/13 **(Item 13 from file: 348)**
DIALOG(R)File 348:EUROPEAN PATENTS

00593835
Computer simulation system and method for specifying the behavior of graphical operator interfaces.
Rechnersimulationssystem und Verfahren zum Spezifizieren vom Verhalten graphischer Bedienerschnittstellen.
Systeme de simulation par ordinateur et methode pour specifier le comportement d'interfaces d'operateur graphiques.
PATENT ASSIGNEE:
VIRTUAL PROTOTYPES, INC., (1707660), 5252 De Maisonneuve West, Suite 318, Montreal, Quebec H4A 3S5, (CA), (applicant designated states: AT;CH;DE;FR;GB;IT;LI;NL;SE)
INVENTOR:
Joseph,Eugene R., 4692 Roslyn Street, Montreal(Quebec), (CA)
Trachtman,Michael, 542 California Street, Newton,Massachusetts 02160, (US)
LEGAL REPRESENTATIVE:
Zeitler & Dickel (101201), Patentanwalte European Patent Attorneys Herrnstrasse 15, D-80539 Munchen, (DE)
PATENT (CC, No, Kind, Date): EP 597316 A2 940518 (Basic)
EP 597316 A3 950816
APPLICATION (CC, No, Date): EP 93117333 931026;
PRIORITY (CC, No, Date): US 972779 921109
DESIGNATED STATES: AT; CH; DE; FR; GB; IT; LI; NL; SE
INTERNATIONAL PATENT CLASS: G06F-009/44;

ABSTRACT EP 597316 A2
A computer simulator system allows the user to specify prototype reaction to events in a pictorial manner using a visual object environment. A spreadsheet like State Table and a visual object collection coincide on a common graphical display. The State Table is

filled in by pointing to lists of events or actions associated with the different objects. The contents of these lists are dependent on the object class. Event or action descriptions are transported into the respective cells of the State Table in the form of descriptive strings of text. This text describes the event or action, and the event source, or action destination. Entries in the State Table define the operation of the simulation and are executed directly by an interpreter or are compiled to generate a program of instructions for performing the simulation.

ABSTRACT WORD COUNT: 137

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	940518	A2	Published application (Alwith Search Report ;A2without Search Report)
Change:	950215	A2	Representative (change)
Search Report:	950816	A3	Separate publication of the European or International search report
Examination:	960228	A2	Date of filing of request for examination: 951222
Examination:	981118	A2	Date of despatch of first examination report: 981005
Withdrawal:	990811	A2	Date application deemed withdrawn: 19990216

LANGUAGE (Publication,Procedural,Application): English; English; English

FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPABF2	1826
SPEC A	(English)	EPABF2	12012
Total word count - document A			13838
Total word count - document B			0
Total word count - documents A + B			13838

...CLAIMS according to claim 1 wherein said state table editor module includes a collection of reaction rules forming a reaction table stored in memory.

4. A **finite state machine** for simulating a system and responsive to a signal representing a **present state** of the simulated system and to a plurality of input signals for deriving an output signal including a signal defining a next state of the simulated system, said **finite state machine** including:

a random access memory responsive to an address signal for selectively retrieving instruction signals stored therein; and

a processing unit for storing the present...

...visual characteristics, and

(iii) changeable features of said displayable visual characteristics responsive to said controlling parameter; describing a state table defining the operation of a **finite** state machine, the state table including

(i) present states of the finite state machine,

(ii) events to be monitored in each of the present states states, and

(iii) next states of the finite state machine in response to detection of a respective event to be monitored in said present **states** ;

operating said finite state **machine** responsive to said state table to display said graphic objects including

(i) defining an instant one of said **present states** of the **finite state machine** defined in said state table.

(ii) detecting an event of the events to be monitored in said instant **present state** ,

(iii) generating a controlling parameter in response to said detected event of said instant **present state** in accordance with said state table, and

(iv) defining a next state of the **finite state machine** in response to said detected event of said instant **present state** in accordance with said state table; and displaying said graphic objects in response to said controlling parameter generated by said generating step.

```
File   8:Ei Compendex(R) 1970-2004/Mar W4
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/Mar
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File 202:Info. Sci. & Tech. Abs. 1966-2004/Feb 27
         (c) 2004 EBSCO Publishing
File  65:Inside Conferences 1993-2004/Apr W1
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File   2:INSPEC 1969-2004/Mar W4
         (c) 2004 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2004/Mar W3
         (c)2004 Japan Science and Tech Corp(JST)
File   6:NTIS 1964-2004/Apr W1
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2004/Mar W4
         (c) 2004 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Apr W1
         (c) 2004 Inst for Sci Info
File 233:Wilson Appl. Sci & Tech Abs 1983-2004/Mar
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File  95:TEME-Technology & Management 1989-2004/Mar W3
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File  62:SPIN(R) 1975-2004/Feb W3
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Set      Items   Description
S1       27151   (STATE OR STATEFUL)()MACHINE? ? OR FINITE()STATE? ?
S2      129916   (CURRENT OR RECENT OR EXISTING OR PRESENT)(1W)(STATE? ? OR
              CONDITION? ?)
S3        6830   (PAST OR PREVIOUS OR PRIOR OR PRECEDING OR LAST OR EARLIER
              OR FORMER)(1W)(STATE? ? OR CONDITION? ?)
S4      261646   (FUTURE OR ALLOWED OR ALLOWABLE OR PERMITTED OR PERMISSIBLE
               OR AUTHORIZED OR AUTHORISED OR ACCEPTED OR ACCEPTABLE OR NOR-
              MAL OR EXPECTED OR RANGE? ?)(5N)(STATE? ? OR CONDITION? ?)
S5        5624   DIGITAL()SIGNATURE? ?
S6       14434   (PUBLIC OR PRIVATE)()KEY? ?
S7      158506   CRYPTO? OR CRYPTANALY? OR CIPHER? OR CYPHER? OR ENCRYPT? OR
               ENCIPHER? OR SCRAMBL? OR DECRYPT? OR DECIPHER? OR UNENCRYPT?
              OR UNSCRAMBL?
S8           4   S1 AND S2:S4 AND S5:S7
S9      121102   AUTHENTICAT? OR SECUR? OR SAFE??
S10      334730   CONTROLLER? ?
S11         114   S1 AND S2:S4 AND S9:S10
S12         114   S8 OR S11
S13          60   RD (unique items)
S14          34   S13 NOT PY=1997:2004
S15          15   S1 AND S2 AND S3:S4
S16           0   S1 AND S3 AND S4
S17          11   RD S15 (unique items)
S18           7   S17 NOT PY=1997:2004
S19           7   S1 AND S5
S20          40   S1 AND S6
S21          46   S19:S20
S22          31   RD (unique items)
S23          16   S22 NOT (PY=1997:2004 OR S14 OR S18)
S24         178   S1 AND S7
S25         122   RD (unique items)
S26          54   S25 NOT (PY=1997:2004 OR S14 OR S18 OR S23)
S27       22958   FINITE()STATE? ?
S28          46   S26 AND S27
S29       12169   S27()(MACHINE? ? OR DEVICE? ? OR UNIT? ?)
S30          30   S26 AND S29
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S31	14	S26 AND S9:S10
S32	20	S30 NOT S31
S33	727	S1 AND S2:S4
S34	20243	S2:S4(10N)(MACHINE? ? OR DEVICE? ? OR UNIT OR UNITS OR HARDWARE OR AUTOMATION OR DESIGN? OR MANUFACTUR? OR ENGINEER?)
S35	201	S33 AND S34
S36	109	S29 AND S35
S37	78	RD (unique items)
S38	44	S37 NOT (PY=1997:2004 OR S14 OR S18 OR S23 OR S31:S32)
S39	460	S29 AND S9
S40	16	S39 AND AUTHENTICAT?
S41	13	RD (unique items)
S42	4	S41 NOT (PY=1997:2004 OR S14 OR S18 OR S23 OR S31:S32 OR S38)
S43	119	S39 AND SECUR?
S44	95	RD (unique items)
S45	19	S44 NOT (PY=1997:2004 OR S14 OR S18 OR S23 OR S31:S32 OR S38 OR S42)

14/5/14 (Item 14 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

[illegible] E.I. Monthly No: EIM8606-040309
Title: **INHERENT DIFFICULTIES IN GLOBALLY OPTIMAL MATERIAL TRANSPORT SCHEDULING WITHIN FLEXIBLE MANUFACTURING SYSTEMS.**
Author: Maletz, Mark C.
Corporate Source: Industrial Technology Inst
Conference Title: 1984 ACM Twelfth Annual Computer Science Conference: The Future of Computing, CSC '84 and SIGCSE Symposium.
Conference Location: Philadelphia, PA, USA Conference Date: 19840214
Sponsor: ACM, New York, NY, USA
E.I. Conference No.: 07112
Source: Publ by ACM, New York, NY, USA p 183
Publication Year: 1984
ISBN: 0-89791-127-X
Language: English
Document Type: PA; (Conference Paper)
Journal Announcement: 8606
Abstract: A major topic in Flexible Manufacturing System research concerns control of the underlying Material Transport System (MTS). This control is typically accomplished by first generating a schedule for the material transportation, and then converting this schedule into instructions that can be executed by the MTS devices (e. g. , programmable **controllers**). A desirable objective of such scheduling is the production of globally optimal schedules and the associated control instructions, where the **current** ' **state** ' of the MTS is consulted and the system is directed to a desired **future** ' **state** '. Unfortunately, this global optimization is inherently difficult from a computational point of view, which may explain why existing systems use less sophisticated scheduling techniques. This talk presents a **Finite State** Automata (FSA) representation of the MTS control problem, and then uses this model to identify computational difficulties involved in global MTS scheduling. The FSA states correspond to 'states' of the MTS, which can be characterized by sensor values and queue-related information. Scheduling in the FSA model generalizes to calculating state transitions to satisfy reachability constraints. A computationally tractable alternative to globally optimal MTS scheduling is then introduced. (Author abstract)
Descriptors: *COMPUTER AIDED MANUFACTURING; COMPUTER PROGRAMMING--Applications; SCHEDULING; INDUSTRIAL PLANTS--Flexible Manufacturing Systems
Identifiers: MATERIAL TRANSPORT SYSTEM; ABSTRACT ONLY
Classification Codes:
723 (Computer Software); 913 (Production Planning & Control)
72 (COMPUTERS & DATA PROCESSING); 91 (ENGINEERING MANAGEMENT)

14/5/15 (Item 15 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01138709 E.I. Monthly No: EI8208067248 E.I. Yearly No: EI82025689
Title: **CONFIDENTIALITY OF INFORMATION.**
Author: Roos, H.
Corporate Source: Klynveld Kraayenhof & Co, Amsterdam, Neth
Source: Information & Management v 4 n 1 Mar 1981 p 17-21
Publication Year: 1981
CODEN: IMANDC ISSN: 0378-7206
Language: ENGLISH
Journal Announcement: 8208
Abstract: The relationship between organization structure, the supporting information systems and the confidentiality issue, defines the end user's responsibility for information control. In a data sharing environment end users must agree upon their mutual responsibility for shared data. The database adminstrator is the natural authority to control the execution of that agreement. Any departure from strictly preventive control weakens data sharing control. On-line end user access control by means of **security** tables may be compromised by the **current** privileged **state machine**

architecture. Resulting control weaknesses should be compensated by procedural and organizational means. 3 refs.
Descriptors: DATA PROCESSING, BUSINESS--* **Security** of Data; INFORMATION DISSEMINATION--Control; MANAGEMENT SCIENCE--Applications
Classification Codes:
723 (Computer Software); 901 (Engineering Profession); 731 (Automatic Control Principles)
72 (COMPUTERS & DATA PROCESSING); 90 (GENERAL ENGINEERING); 73 (CONTROL ENGINEERING)

14/5/16 **(Item 1 from file: 35)**
DIALOG(R)File 35:Dissertation Abs Online
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01499585 ORDER NO: AAD97-02953
INTERLEAVING PLANNING AND EXECUTION
Author: NOURBAKHSH, ILLAH REZA
Degree: PH.D.
Year: 1996
Corporate Source/Institution: STANFORD UNIVERSITY (0212)
Adviser: MICHAEL R. GENESERETH
Source: VOLUME 57/08-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 5161. 148 PAGES
Descriptors: COMPUTER SCIENCE
Descriptor Codes: 0984

In this dissertation, we explore architectures and termination criteria for interleaving planning and execution. Our aim is to present a broad study of interleaving, describing approaches that allow **safe** , early termination of planning episodes and corresponding control systems that achieve specified goal conditions cheaply by taking advantage of the gains incurred through interleaving.
We intend to describe a basic control architecture for controlling multiple planning and execution episodes. Furthermore, we will describe planning termination criteria. The criteria will be based on a variety of techniques, from the analysis of the structure of candidate plans to the creation of abstraction systems that "direct" early termination of ground-level planning. We will **present conditions** under which theoretical results of soundness, completeness and optimality hold for our techniques. In addition, we will describe long-term empirical results with simulation and real-world mobile robot tests. Finally, throughout this work we also hope to show that many of the current results in the action planning, **finite state machine** learning, and mobile robot navigation communities are special cases of the more general systems and termination criteria presented here.

14/5/17 **(Item 2 from file: 35)**
DIALOG(R)File 35:Dissertation Abs Online
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01499585 ORDER NO: AADNN-08167
LOGIC CONTROL: MARKOVIAN FRAGMENTS, HIERARCHY AND HYBRID SYSTEMS (COCOLOG)
Author: WEI, YUAN-JUN
Degree: PH.D.
Year: 1995
Corporate Source/Institution: MCGILL UNIVERSITY (CANADA) (0781)
Adviser: PETER E. CAINES
Source: VOLUME 57/04-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 2779. 177 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0544
ISBN: 0-612-08167-2

Based upon the COCOLOG (Conditional Observer and **Controller** Logic) control formalism, we present a framework, called a system of environments, which permits efficient updating of the axiom sets of

a COCOLOG system. The key idea is that one should only retain those axioms and theorems concerning the most **recent state** estimate of the controlled machine. This information is sufficient to evaluate the truth of conditional control formulas which only depend upon the **current state** estimate of the controlled machine. As a result, a Markovian fragment system is demonstrated to have virtually the same control power as a full COCOLOG system. Further, it is shown that a Markovian fragmented system has a complexity of logical deduction which is time-dependent while a full COCOLOG system has a complexity which increases monotonically with time.

In order to formulate the analysis and synthesis of hierarchical systems, a hierarchical structure based upon the notion of dynamical consistency is presented. The underlying motivation for this notion is that high level dynamics should be consistent with low level dynamics. The major part of this investigation is carried out for the so-called in-block controllable partition lattices, which are the lattices of partitions for which each block element constitutes a controllable submachine. We show that most controllable **finite state machines** have at least one non-trivial in-block controllable partition machine. It is also shown that, subject to in-block controllability, the resulting partition machines are controllable if and only if the base machines are controllable. A consequence of this construction is that a state-to-state reachability problem can be decomposed into reachability problems at different levels of abstraction. In terms of this theory, a hierarchical control system is a set of control systems associated with a chain from the top element to the bottom element of the in-block controllable partition lattice of a controlled machine.

As an extension of regular COCOLOG, we give the HICOLOG formulation of hierarchical logic control. The basic contribution is the construction of a system wherein a high level logic **controller** makes its control decisions with respect to the information available to it and communicates its commands as control objectives to the associated low level logic control systems; this is continued down the chain of systems in a given hierarchical lattice. Information flows up the hierarchy in the form of abstract statements concerning the system state.

The notion of dynamical consistency is extended to hybrid systems so as to define the set of dynamically consistent hybrid partition machines associated with a continuous system ${\cal S}$. It is shown that it is possible to define an in-block controllable hybrid partition lattice for ${\cal S}$ and this permits the hybrid control of a continuous system ${\cal S}$ to be formulated within a lattice theoretic hierarchical control theory.

14/5/18 (Item 3 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

7027223 ORDER NO: AAD88-24208
THE ARCHITECTURE AND IMPLEMENTATION OF MEMNET: A HIGH-SPEED SHARED-MEMORY COMPUTER COMMUNICATION NETWORK
Author: DELP, GARY SCOTT
Degree: PH.D.
Year: 1988
Corporate Source/Institution: UNIVERSITY OF DELAWARE (0060)
PROFESSOR IN CHARGE: DAVID J. FARBER
Source: VOLUME 49/08-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 3292. 270 PAGES
Descriptors: COMPUTER SCIENCE; ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0984; 0544

A major limitation of current distributed system technology is that the overhead associated with the normal input/output paradigm of interconnection severely affects the system performance. This research has taken a new perspective on the interconnection problem based on a memory extension paradigm. Evidence to date demonstrates that the processor overhead is greatly reduced and significant additional functionality is gained.

Memnet is a computer architecture in which the local network appears

as memory in the physical address space of each processor on the network. Local area networking and distributed system support are two potential applications of this architecture. The Memnet principles of computer/communication interconnection are extendable to wide-area, high-speed, low-latency processor interconnection.

This dissertation includes a survey of interprocess communication schemes and shared memory architectures. A description of the Memnet architecture and implementation is followed by an analysis of the behavior of the Memnet architecture over a wide **range** of uses. The **state machines** and schematics of the experimental implementation are included as appendices.

Analytic and experimental results confirm the viability of distributed shared memory supported in hardware at the memory **controller** level. For many applications, the impact of distributing the memory resource is under [illegible] the undistributed performance.

14/5/19 **(Item 1 from file: 202)**
DIALOG(R)File 202:Info. Sci. & Tech. Abs.
(c) 2004 EBSCO Publishing. All rts. reserv.

1603131
Confidentiality of information.
Author(s): Roos, H
Corporate Source: Klynveld Kraayenhof & Co., Amsterdam, Netherlands
Information Management Review vol. 9, no. 1, pages 17-21
Publication Date: Mar 1981
ISSN: 0961-7612
Language: English
Document Type: Journal Article
Record Type: Abstract
Journal Announcement: 1600

The relationship between organization structure, the supporting information systems and the confidentiality issue, defines the end user's responsibility for information control. In a data sharing environment end users must agree upon their mutual responsibility for shared data. The database administrator is the natural authority to control the execution of that agreement. Any departure from strictly preventive control weakens data sharing control. On-line end user access control by means of **security** tables may be compromised by the **current** privileged **state machine** [illegible]. Resulting control weaknesses should be compensated by [illegible] organizational means.

[illegible] Codes and Description: 2.00 (General Aspects)
[illegible] Reading: Research Methods

14/5/20 **(Item 1 from file: 2)**
DIALOG(R)File 2:INSPEC
(c) 2004 Institution of Electrical Engineers. All rts. reserv.

5526626 INSPEC Abstract Number: C9704-1340G-015
Title: On optimization of a class of hybrid systems with fast stochastic dynamics
Author(s): Altman, E.; Gaitsgory, V.; Shi, P.
Author Affiliation: Inst. Nat. de Recherche en Inf. et Autom., Sophia Antipolis, France
Conference Title: Proceedings of the 35th IEEE Conference on Decision and Control (Cat. No.96CH35989) Part vol.1 p.523-8 vol.1
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA 4 vol. 4858 pp.
ISBN: 0 7803 3590 2 Material Identity Number: XX96-03111
U.S. Copyright Clearance Center Code: 0 7803 3590 2/96/$5.00
Conference Title: Proceedings of 35th IEEE Conference on Decision and Control
Conference Sponsor: IEEE Control Syst. Soc.; Soc. Instrum. & Control Eng. ; Inst. Syst., Control & Inf. Eng

Conference Date: 11-13 Dec. 1996 Conference Location: Kobe, Japan
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: We consider the problem of control for continuous time stochastic hybrid systems in finite time horizon. The systems considered are nonlinear: the state evolution is a nonlinear function of both the control and the state. The control parameters change at discrete times according to an underlying controlled Markov chain which has **finite** state and action spaces. The objective is to design a **controller** which minimizes an **expected** nonlinear cost of the **state** trajectory. We show, using an averaging procedure, that the above minimization problem can be approximated by the solution of some deterministic optimal control problem. This paper generalizes our previous results obtained for systems whose state evolution is linear in the control. (22 Refs)
Subfile: C
Descriptors: continuous time systems; control system synthesis; discrete time systems; Markov processes; minimisation; optimal control; stochastic systems
Identifiers: hybrid systems; fast stochastic dynamics; continuous time stochastic hybrid systems; finite time horizon; state evolution; nonlinear function; controlled Markov chain; expected nonlinear cost; state trajectory; averaging proced; minimization problem; deterministic optimal control problem
Class Codes: C1340G (Time-varying control systems); C1180 (Optimisation techniques); C1330 (Optimal control); C1310 (Control system analysis and synthesis methods); C1340D (Discrete control systems); C1140Z (Other topics in statistics)

14/5/21 (Item 2 from file: 2)

4974079 INSPEC Abstract Number: C9507-7420D-010
Title: The principles of state logic control
Author(s): Chambers, W.
Author Affiliation: Adatek Inc., Sandpoint, ID, USA
Conference Title: Proceedings of the Industrial Computing Conference. ICS/94 p.119-30
Publisher: ISA, Research Triangle Park, NC, USA
Publication Date: 1994 Country of Publication: USA xiii+410 pp.
U.S. Copyright Clearance Center Code: 1058-8655/94/119-130/$0+.50pp
Conference Title: Proceedings of the Industrial Computing Conference. ICS/94
Conference Date: 23-28 Oct. 1994 Conference Location: Anaheim, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: State logic control is rapidly growing in popularity with most of the major venders offering some form of state logic control strategy. There have been thousands of products sold in this country to large and small customers alike. Over half of all new control installations in Europe are now implemented using state logic. Traditional control strategies have a long history based on hardwired or non electrical solutions of the **past**. **State** logic is based on **Finite State Machine** Theory which allows the computer to more closely mirror the real world application. State logic's primary elements are tasks which are composed of one or more states. Tasks all execute simultaneously or in parallel with one state active at a time. The logic in the non-active states is ignored making state logic naturally more efficient. Besides simplifying control, state logic's special capabilities include diagnostics, data handling, and the ability to add special high level tools for the user. State logic empowers the user. Its objective is to become transparent, allowing clear focus on control system design. State logic significantly shortens the distance between the logical and clever thinking of the engineer and the final control program and permits the factory floor smarts of the maintenance technician to be applied directly and effectively to getting processes and machines commissioned quickly and increasing uptime over time. (0 Refs)

Subfile: C
Descriptors: control system CAD; **finite state machines** ; high level [illegible]; process control; programmable **controllers**
Identifiers: state logic control; **finite state machine** theory; [illegible] systems level process diagnostics; data handling
Class Codes: C7420D (Control system design and analysis); C3220B (Programmable controllers); C3350 (Control in industrial production systems); C3355 (Control applications in manufacturing processes); C4220 (Automata theory); C6140D (High level languages); C1310 (Control system analysis and synthesis methods)

14/5/22 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

[illegible] INSPEC Abstract Number: C9408-5210B-001
Title: **Automatic synthesis of self-clocked asynchronous** state machines **and parallel** controllers
Author(s): Aghdasi, F.
Author Affiliation: Dept. of Electr. Eng., Zimbabwe Univ., Harare, Zimbabwe
Journal: Applied Mathematics and Computer Science vol.4, no.1 p. 139-52
Publication Date: 1994 Country of Publication: Poland
ISSN: 0867-857X
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Classical methods for the design of asynchronous **state machines** are usually complicated, due to critical races and hazards, and necessitate special state assignment techniques and hazard-free combinational logic, leading to extra hardware. The necessity for such special considerations prevents asynchronous designs from taking advantage of the CAD tools developed for synchronous machines. This paper presents a novel approach to such designs, which enables asynchronous **state machines** to be systematically synthesized with minimum state variables and arbitrary **state** encoding. Multiple input changes are **allowed** . The method uses a separate data-driven clock for each state variable. The combinational logic is hazard-free by default, allowing flexibility of minimization. Mealy-Moore outputs can be generated without hazards. Simple latches in a master-slave configuration are used as memory elements, rendering the method suitable for implementation in SSI or VLSI. The method [illegible] the use of extra delay elements, which are often necessary in [illegible] circuits. The simplicity of this method enables the design [illegible] to be derived directly from the algorithmic **state machines** [illegible] than from flow tables. The method is illustrated by its application [illegible] the design of a VMEbus requester. The methodology is then extended to parallel **controllers** represented by Petri nets, and is automated using state assignment techniques that have already been developed for synchronous parallel **controllers** . (23 Refs)
Subfile: C
Descriptors: asynchronous sequential logic; clocks; flip-flops; hazards and race conditions; logic CAD; minimisation; peripheral interfaces; Petri nets; sequential machines; state assignment; system buses
Identifiers: self-clocked asynchronous **state machines** ; asynchronous parallel **controllers** ; automatic synthesis; state variables; arbitrary state encoding; multiple input changes; data-driven clock; hazard-free combinational logic; minimization flexibility; Mealy-Moore outputs; latches ; master-slave configuration; memory elements; SSI; VLSI; design equations; algorithmic **state machines** ; VMEbus requester; Petri nets; state assignment techniques; CAD
Class Codes: C5210B (Computer-aided logic design); C1180 (Optimisation techniques); C5120 (Logic and switching circuits); C4230D (Sequential switching theory); C5610S (System buses); C4220 (Automata theory); C5610P (Peripheral interfaces); C7430 (Computer engineering)

14/5/23 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

4446095 INSPEC Abstract Number: B9308-6150M-018, C9308-5640-022
Title: A verification procedure via invariant for extended communicating finite - state machines
Author(s): Higuchi, M.; Shirakawa, O.; Seki, H.; Fujii, M.; Kasami, T.
Author Affiliation: Dept. of Inf. & Comput. Sci., Osaka Univ., Toyonaka, Japan
Conference Title: Computer Aided Verification. Fourth International [illegible], CAV '92. Proceedings p.384-95
Editor(s): Bochmann, G.v.; Probst, D.K.
Publisher: Springer-Verlag, Berlin, Germany
Publication Date: 1993 Country of Publication: West Germany ix+422 pp.
ISBN: 3 540 56496 9
Conference Date: 29 June-1 July 1992 Conference Location: Montreal, Que., Canada
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: This paper presents a method for verifying **safety** property of a communication protocol modeled as two extended communicating **finite - state machines** with two unbounded FIFO channels connecting them. In this method, four types of atomic formulae specifying a condition on a machine and a condition on a sequence of messages in a channel are introduced. A human verifier describes a logical formula which expresses **conditions expected** to be satisfied by all reachable global states, and a verification system proves that the formula is indeed satisfied by such states (i.e. the formula is an invariant) by induction. If the invariant is never satisfied in any unsafe state, it can be concluded that the protocol is **safe** . To show the effectiveness of this method, a sample protocol extracted from the data transfer phase of the OSI session protocol was verified by using the verification system. (14 Refs)
Subfile: B C
Descriptors: **finite state machines** ; formal verification; open systems; protocols
Identifiers: verification procedure; invariant; extended communicating finite - **state machines** ; **safety** property; communication protocol; FIFO channels; atomic formulae; human verifier; reachable global states; data transfer phase; OSI session protocol
Class Codes: B6150M (Protocols); C5640 (Protocols); C4230 (Switching theory); C4220 (Automata theory)

14/5/24 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

04358552 INSPEC Abstract Number: C9304-6140D-025
Title: Proving specifications of tasking systems using Ada/TL
Author(s): Peters, J.; Hankley, W.
Author Affiliation: Dept. of Comput. & Inf. Sci., Kansas State Univ., Manhattan, KS, USA
Conference Title: Proceedings TRI-Ada '90 p.4-13
Publisher: ACM, New York, NY, USA
Publication Date: 1990 Country of Publication: USA xxvi+630 pp.
ISBN: 0 89791 409 0
U.S. Copyright Clearance Center Code: 0 89791 409 0/90/1200-4$1.50
Conference Sponsor: ACM
Conference Date: 3-7 Dec. 1990 Conference Location: Baltimore, MD, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Ada/TL is a language for specification of the behaviour of systems of communicating tasks. It merges concepts of the specification [illegible] Ada, VDM specification of packages, and temporal logic [illegible] specification of task behavior. The TL part consists of constructive [illegible] specification of behaviors of individual tasks and a system specification

of the properties of the interaction of tasks. The authors extend earlier work on proof of system specifications (W. Hankley, J. Peters, 1990) to cover more general branching behaviours of individual tasks, including cases of timed task calls and timed rendezvous. The constructive specification of each individual task defines a **finite state** computation model of its possible behaviors with allowed communications between task computations. The proof system uses marker symbols to represent the **current state** within each task computation, inference rules to justify transformations from one state to the next, and a proof tableau for representing the proof steps. The method rests upon the technique of using an invariant system property to identify a finite computation model of the interaction of all the system tasks. The proof method is illustrated using an example of a traffic walk-light **controller** with a timed behavior. (22 Refs)

Subfile: C

Descriptors: Ada; formal specification; specification languages; temporal logic; theorem proving; Vienna development method

Identifiers: Ada/TL; communicating tasks; VDM specification; temporal logic specification; task behavior; constructive specification; individual tasks; system specification; general branching behaviours; timed task calls ; timed rendezvous; **finite state** computation model; allowed communications; marker symbols; inference rules; proof tableau; proof steps ; invariant system property; finite computation model; system tasks; traffic walk-light **controller**

Class Codes: C6140D (High level languages); C6110B (Software engineering techniques); C4210 (Formal logic)

14/5/25 (Item 6 from file: 2)

INSPEC Abstract Number: B9201-1265B-059, C9201-5210-027

Title: **Automatic synthesis of a dual-PLA** controller **with a counter**

Author(s): Binger, D.; Knapp, D.W.

Author Affiliation: Dept. of Comput. Sci., Illinois Univ., Chicago, IL, USA

Conference Title: Proceedings of the 23rd Annual Workshop and Symposium. MICRO 23. Microprogramming and Microarchitecture (Cat. No.90TH0341-8) p. 149-57

Publisher: IEEE Comput. Soc. Press, Los Alamitos, CA, USA

Publication Date: 1990 Country of Publication: USA x+299 pp.

ISBN: 0 8186 2124 9

U.S. Copyright Clearance Center Code: 0194-1895/90/0000/0149/$01.00

Conference Sponsor: IEEE; ACM

Conference Date: 27-29 Nov. 1990 Conference Location: Orlando, FL, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: When datapath/ **controller** designs are synthesized from high-level specifications, the control state graph can have hundreds of states and a large number of state transitions which depend only on the **present state** . For this class of **finite state machines** , an implementation with two PLAs and a counter can have much less area than a single-PLA implementation. This paper presents a new automatic procedure for coding the internal variables of an FSM with two PLAs and a counter in which the codes are selected to reduce the size of both PLAs. Analysis of the results shows that for a broad class of large FSMs the authors circuits have less cost than can be obtained using previously published automatic synthesis procedures. (13 Refs)

Subfile: B C

Descriptors: counting circuits; finite automata; logic arrays; logic design; microcontrollers

Identifiers: automatic synthesis; datapath design; dual-PLA **controller** ; counter; high-level specifications; control state graph; state transitions; **finite state machines** ; coding; internal variables

Class Codes: B1265B (Logic circuits); B1265F (Microprocessors and microcomputers); C5210 (Logic design methods); C4220 (Automata theory); C5130 (Microprocessor chips)

14/5/26 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC
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03305405 INSPEC Abstract Number: B89008544, C89012970
Title: Stand-alone microsequencer (SAM) implements high-performance state machines
Author(s): Kopec, S.
Author Affiliation: Altera Corp., Santa Clara, CA, USA
Conference Title: Northcon/87. Conference Record p.6/3/1-4
Publisher: Electron. Conventions Manage, Los Angeles, CA, USA
Publication Date: 1987 Country of Publication: USA 612 pp.
Sponsor: IEEE; ERA; Electron. Manuf. Assoc
Conference Date: 22-24 Sept. 1987 Conference Location: Portland, OR, USA
Availability: Western Periodicals Co., North Hollywood, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); Practical (P); Product Review (R)
Abstract: The **current state** -of-the-art in **state machine** and **controller** design is represented by the Stand-alone Microsequencer, or SAM, concept implemented in the EPS448 device. This device, implemented in an advanced 1 micron CMOS, EPROM technology, offers the benefits of high density (448*36 Microcode store on-chip), low CMOS power (less than half a Watt), high-performance (30 MHz operation), and EPROM reprogrammability. [illegible] diagram of the SAM device is shown. The device has two major components, one the Microcoded Engine, and the other the EPLD Branch Control logic. (0 Refs)
Subfile: B C
Descriptors: CMOS integrated circuits; EPROM; logic arrays; microprocessor chips
Identifiers: Altera; high-performance **state machines** ; Stand-alone Microsequencer; SAM; EPS448; CMOS; EPROM; high density; Microcode store on-chip; EPROM reprogrammability; block diagram; Microcoded Engine; EPLD Branch Control logic
Class Codes: B1265F (Microprocessors and microcomputers); B1265B (Logic circuits); B2570D (CMOS integrated circuits); B1265D (Memory circuits); C5130 (Microprocessor chips); C5120 (Logic and switching circuits); [illegible] (Semiconductor storage)

14/5/27 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC
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02969876 INSPEC Abstract Number: B87059070, C87055816
Title: Second-generation compilers optimize semicustom circuits
Author(s): Rowson, J.; Trimberger, S.
Author Affiliation: VLSI Technol. Inc., San Jose, CA, USA
Journal: Electronic Design vol.35, no.4 p.92-6
Publication Date: 19 Feb. 1987 Country of Publication: USA
CODEN: ELODAW ISSN: 0013-4872
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Product Review (R)
Abstract: By accepting high-level specifications and translating designs into either a fully custom layout or a net list for a gate-array chip or standard-cell block, a new generation of compilers optimizes circuitry for the chip type chosen. The first members of the second-generation family are a data path and a **state machine** compiler. The new compilers were co-developed by VLSI Technology and design engineers from Rockwell International. The programs are written in Xidak Inc.'s Mainsail. The second-generation data-path version supplies logic that operates on multibit data in a bus architecture. The compiler does not limit the number of buses or type of clocking in the data path. The resulting data path [illegible] a natural processor-data section, and the multibit logic is also [illegible] systems such as computer peripherals, digital signal processing [illegible] graphics **controllers** . The **state machine** compiler builds a

circuit with outputs and an internal state that depend on the inputs and **current** internal **state** . A clock pulse changes the outputs and internal state. This circuit offers a simple way to generate logic for 1-bit data. (0 Refs)
Subfile: B C
Descriptors: circuit layout CAD; logic CAD; software packages
Identifiers: second-generation silicon compilers; data path compiler; [illegible] circuits; fully custom layout; net list; gate-array chip; [illegible]-level block; **state machine** compiler; VLSI Technology; Rockwell International
Class Codes: B1130B (Computer-aided circuit analysis and design); B1265 (Digital electronics); C5210B (Computer-aided logic design); C7410D (Electronic engineering)

14/5/28 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

02202450 INSPEC Abstract Number: C84012603
Title: A nonvolatile store or system state
Author(s): Chita, J.S.
Journal: Electronic Engineering vol.56, no.685 p.34
Publication Date: Jan. 1984 Country of Publication: UK
CODEN: ELCEA9 ISSN: 0013-4902
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Practical (P)
Abstract: Discusses an important concept for a fault tolerant real-time computer system (with respect to power transients)-the need for a nonvolatile store to hold the system state so that after a power transient (micro-secs) the system can recover to its **previous state** without having to go through a cold start sequence as is usual in an industrial control system. It is also useful in **state machine** concept software systems and computers working on concepts of error recovery rollback points, where at certain milestones the machine state is written to store and subsequently if an error occurs the system can retry from the last milestone point. (0 Refs)
Subfile: C
Descriptors: digital storage; fault tolerant computing; **security** of data
Identifiers: system state; fault tolerant real-time computer system; power transients; nonvolatile store; **state machine** concept software; error recovery rollback points
Class Codes: C5320 (Digital storage)

14/5/29 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02615251 JICST ACCESSION NUMBER: 96A0206829 FILE SEGMENT: JICST-E
A Method for Constructing Self-Stabilizing Communication Protocols modeled as 2-ECFSMs.
KATAKURA KEN'ICHI (1); HIGUCHI MASAHIRO (1); FUJII MAMORU (1)
(1) Osaka Univ., Fac. of Eng. Sci.
Joho Shori Gakkai Kenkyu Hokoku, 1996, VOL.96,NO.12(DPS-74 GW-15), PAGE.13-18, FIG.2, REF.5
JOURNAL NUMBER: Z0031BAO ISSN NO: 0919-6072
UNIVERSAL DECIMAL CLASSIFICATION: 681.32+ 621.394/.395
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: For implementing reliable communication systems, it is important to design communication protocols considering faults. In this paper, we propose a method in which, self-stabilizing protocols are constructed based on communication protocols which are shown to be **safe** on the assunmption that no faults occur in 2-ECFSM model. In proposing method,

protocols are extended to be able to recover from every deadlock state or unspecified reception state to a **safe** state by adding some action. To such a **safe** state, a state is chosen so that it is the closest to **current state** among all **safe** states. For such a purpose, we define a distance between two states in a protocol, and discuss some properties that hold on the notion. (author abst.)
DESCRIPTORS: fault tolerance; telecommunication; protocol; system model; deadlock; stabilization; **finite state machine** ; communication system model; restoration; crash recovery
BROADER DESCRIPTORS: resistance(endure); rule; model; modification; sequential machine; automaton
CLASSIFICATION CODE(S): JC02050G; ND11010T

14/5/30 **(Item 2 from file: 94)**
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1419682 JICST ACCESSION NUMBER: 92A0111678 FILE SEGMENT: JICST-E
A Verification System for Communication Protocols Modeled as Extended Communicating Finite - State Machines .
SHIRAKAWA OSAMU (1); HIGUCHI MASAHIRO (1); SEKI HIROYUKI (1); FUJII MAMORU (2); KASAMI TADAO (2)
(1) Osaka Univ., Faculty of Engineering Science; (2) Osaka Univ., College of General Education
Joho Shori Gakkai Kenkyu Hokoku, 1991, VOL.91,NO.106(SE-82), PAGE.87-94, FIG.6, TBL.6, REF.9
JOURNAL NUMBER: Z0031BAO ISSN NO: 0919-6072
UNIVERSAL DECIMAL CLASSIFICATION: 681.3.02.001 681.3.01
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: This paper presents a method for verifying some **safety** properties of a communication protocol modeled as two extended **finite - state machines** with two unbounded FIFO channels connecting them. In our method, four types of atomic formulas specifying a condition on a machine and a condition on a sequence of messages in a channel are introduced. A human verifier describes a logical formula as **conditions expected** to be satisfied by all reachable global states, and a verification system proves that the formula is indeed satisfied by such states (i.e. the formula is an invariant) by induction. If the invariant is not satisfied in any unsafe state, it can be concluded that the protocol is **safe** . To show the effectiveness of our method, we verified some parts of the OSI session protocol using the verification system. (author abst.)
DESCRIPTORS: protocol; **finite state machine** ; program verification; software engineering; program theory; modeling; deadlock; proof(evidence); register
BROADER DESCRIPTORS: rule; sequential machine; automaton; verification; engineering; computation theory; theory; operation(processing)
CLASSIFICATION CODE(S): JD02010R; JB02000A

14/5/31 **(Item 1 from file: 34)**
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05350011 Genuine Article#: VR526 Number of References: 11
Title: **HIGH-PERFORMANCE 2-PHASE MICROPIPELINE BUILDING-BLOCKS - DOUBLE EDGE-TRIGGERED LATCHES AND BURST-MODE SELECT AND TOGGLE CIRCUITS**
Author(s): YUN KY; BEEREL PA; ARCEO J
Corporate Source: UNIV CALIF SAN DIEGO,DEPT ELECT & COMP ENGN,9500 GILMAN DR/LA JOLLA//CA/92093; UNIV SO CALIF,DEPT EE SYST/LOS ANGELES//CA/90089
Journal: IEE PROCEEDINGS-CIRCUITS DEVICES AND SYSTEMS, 1996, V143, N5 (OCT) , P282-288
ISSN: 1350-2409
Language: ENGLISH Document Type: ARTICLE

Geographic Location: USA
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC
Abstract: New high-performance building blocks for two-phase micropipelines are presented, and pseudo-static Svensson-style double edge-triggered D-flip-flogs (DETDFF) for datapath storage are developed in place of traditional capture-pass or transmission gate latches. A DETDFF buffer implementation is compared the **current state** -of-the-art micropipeline implementation using four-phase **controllers** designed by Day and Woods for the AMULET-2 processor and also with Sutherland's original two-phase micropipeline. All three designs were simulated in the MOSIS 1.2 mu m CMOS process under the worst-case process corner with a 4.6 V power supply and at 100 degrees C. The authors' SPICE simulations show that the DETDFF design has 70% and 150%, higher throughput than Day acid Woods' and Sutherland's, respectively. This higher throughout is due to latching the data on both edges of the latch control. removing the need for a react phase and simplifying the control structures. In addition, two commonly used micropipeline event-control structures, the select and toggle elements, are implemented using the extended-burst-mode 3D synthesis system. Detailed simulations demonstrate that ow implementations are up to 50% faster than traditional implementations. This speed advantage call be primarily attributed to careful applications of generalised C-elements rather than discrete basic gates.
Descriptors--Author Keywords: ASYNCHRONOUS CIRCUITS ; MICROPIPELINES
Research Fronts: 94-0434 002 (NONDETERMINISTIC **STATE MACHINES** IN PROTOCOL CONFORMANCE TESTING; ASYNCHRONOUS INTERFACE CIRCUITS; TIMED PETRI NETS; AUTOMATED MANUFACTURING SYSTEMS)
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YUN KY, 1992, P576, P INT C COMP AID DES

14/5/32 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

05304081 Genuine Article#: VP133 Number of References: 15
Title: **A UNIFIED APPROACH TO FAULT-TOLERANCE IN COMMUNICATION PROTOCOLS BASED ON RECOVERY PROCEDURES**
Author(s): AGARWAL A; ATWOOD JW
Corporate Source: POSITRON FIBER SYST/MONTREAL/PQ/CANADA/; CONCORDIA UNIV,DEPT ELECT & COMP ENGN/MONTREAL/PQ H3G 1M8/CANADA/; CONCORDIA UNIV,DEPT COMP SCI/MONTREAL/PQ H3G 1M8/CANADA/
Journal: IEEE-ACM TRANSACTIONS ON NETWORKING, 1996, V4, N5 (OCT), P785-795
ISSN: 1063-6692
Language: ENGLISH Document Type: ARTICLE
Geographic Location: CANADA
Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences
Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC; COMPUTER SCIENCE, HARDWARE & ARCHITECTURE
Abstract: This paper addresses the problem of fault tolerance in computer communication protocols, modeled by communicating **finite state machines** , by providing an efficient algorithmic procedure for recovery in such systems, Even when the communication network is reliable and maintains the order of messages, any kind of transient errors that may not be detected immediately could contaminate the system resulting in

protocol failure, To achieve fault-tolerance, the protocol must be able to detect the error, and then it must recover from that error and eventually reach a legal (or consistent) **state** , and resume its **normal** execution, A protocol that possesses the latter feature of recovering and continuing its execution starting from a legal state is also called a self-stabilizing protocol, Our recovery procedure does not require the application of an intrusive checkpointing procedure. The stable storage requirement for each process is less than that required for other proposed recovery procedures since volatile storage is used for logging the application messages, The recovery procedure provides us with a legal protocol state, which is the global state before reaching any illegal state and before the effects of the error make other states illegal, Only a minimal number of processes affected by error propagation are required to rollback. Our recovery procedure can be used to recover from any number of transient errors in the system, Our recovery procedure has also been modeled in PROMELA, a language to describe validation models, which shows the syntactic correctness of our recovery protocol design, Finally, our procedure is compared with the existing approaches of handling the errors, and an illustrative example is provided.

Identifiers--KeyWords Plus: SYSTEM; DESIGN

Research Fronts: 94-1454 001 (DISTRIBUTED REAL-TIME SYSTEMS; EFFICIENT ALGORITHM; **SAFETY** -CRITICAL SOFTWARE; MULTIPLE MUTUAL EXCLUSION)

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14/5/33 (Item 3 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

[illegible]302 Genuine Article#: MT511 Number of References: 15

Title: **EVENT-BASED VERIFICATION OF SYNCHRONOUS, GLOBALLY CONTROLLED, LOGIC DESIGNS AGAINST SIGNAL FLOW-GRAPHS**

Author(s): VANAELTEN FV; ALLEN J; DEVADAS S

Corporate Source: INTERUNIV MICROELECTR CTR/B-3001 LOUVAIN//BELGIUM/; MIT,DEPT ELECT ENGN & COMP SCI,ELECTR RES LAB/CAMBRIDGE//MA/02139

Journal: IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, 1994, V13, N1 (JAN), P122-134

ISSN: 0278-0070

Language: ENGLISH Document Type: ARTICLE

Geographic Location: BELGIUM; USA

Subfile: SciSearch; CC ENGI--Current Contents, Engineering, Technology & Applied Sciences

Journal Subject Category: COMPUTER SCIENCE, HARDWARE & ARCHITECTURE

Abstract: We address the problem of automatically verifying large digital designs at the logic level, against high-level specifications. We present a technique which allows for the verification of a:specific class of systems, namely systems with synchronous globally timed control. To a first approximation, these are systems where a single **controller** directs the data through the data path and decides (globally) when to move the data. We address the verification of these systems against a Signal Flow Graph (SFG) specification, or a specification in an applicative language such as SILAGE. In this paper,

a method is presented for verifying the implementation against an intermediate SFG, which is an expansion of the original specification in such a way that all the operations correspond to Register Transfers (RT's) in the implementation. In this SFG, complex arithmetic operations such as multiplications may have been decomposed into simpler ones, such as shifts and additions, and new operations may have been introduced for maintaining iteration indices and computing addresses of memory locations.

SFG's can be viewed as maximally parallel synchronous machines. [illegible] the implementation and the specification are then **Finite State Machines** , having string functions (input/output mappings) associated [illegible]. Correctness is taken to mean that a certain relation (the [illegible]ation) holds between these string functions. This relation extends beyond strict input/output equivalence, and provides room for various behavioral transformations. We **present** sufficient **conditions** for the validity of the beta-relation between the implementation and the expanded SFG. These conditions can be verified automatically and efficiently. They consist of the combinational correctness of data path hardware, and the validity of a number of past-tense Computation Tree Logic (CTL) formulae expressing constraints on control events. The latter can be verified using **Finite State Machine** (FSM) traversal algorithms. In this way, the verification of the composite machine is reduced to the separate verification of the data path and the **controller** . It remains to be shown, after application of our verification procedure, that the expanded SFG is in beta-relation with the original SPG. Experimental results are presented.

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14/5/34 (Item 1 from file: 95)

00723434 E93114349007

Trustable computing in next-generation avionic architectures

(Verlaessliche Berechnung in Avionikarchitekturen der naechsten Generation)

Maughan, WD
Dep. of Defense, USA

8th Annual Computer Security Applications Conf., San Antonio, USA, Nov. 30 - Dec. 4, 19921992
Document type: Conference paper Language: English
Record type: Abstract
ISBN: 0-8186-3115-5; 0-8186-3117-1

ABSTRACT:
In tomorrow's 'brilliant' weapons, next-generation avionic computers will need to orchestrate the actions of many subsystems while further [illegible]aining the **security** of sensitive data, the integrity of key data and [illegible]. behavior, and often other key properties. Maintenance of these [illegible]s will help ensure that system execution is trustable, conforming [illegible] prescribed policies and expected behavior. For traditional **security** (confidentiality) as required by DoD, the policy to be maintained

is well understood and essentially application independent. Although the weapon environment will surely render inadequate much of current **security** engineering practice and likely stress the **security** technology base, the familiar, fundamental mechanisms of MAC and DAC will still form the foundation of suitable multi-level **security** (MLS) maintenance. For integrity maintenance, however, realistic policies are quite application dependent. In general, a specific integrity policy needs to comprehend not only certain behavioral aspects of the overall application, but also of potentially many distinct states within the application. Thus, integrity maintenance requires control derived from a **state machine** specifying ' **acceptable** ' application behavior.

31/5/3 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01201968 ORDER NO: NOT AVAILABLE FROM UNIVERSITY MICROFILMS INT'L.
VLSI DESIGN METHODOLOGIES FOR APPLICATION-SPECIFIC CRYPTOGRAPHIC **AND ALGEBRAIC SYSTEMS**
Author: VERBAUWHEDE, INGRID MARIA ROSA
Degree: PH.D.
Year: 1991
Corporate Source/Institution: KATHOLIEKE UNIVERSITEIT LEUVEN (BELGIUM) (5605)
Source: VOLUME 53/01-C OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 161. 245 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0544
Location of Reference Copy: IMEC-VSDM, KAPELDREEF 75, B-3001 HEVERLEE, BELGIUM

This Ph.D. dissertation describes several new methods for the design of an ASIC (Application Specific Integrated Circuit). These contributions can be situated at several levels of abstract in the design trajectory.

At the specification level, a formal classification of the types of specifications needed for an ASIC implementation is made. It is illustrated by means of the description of the specifications of a **cryptographic** co-processor, which contains a large set of programmable **cryptographic** functions built upon the Data **Encryption** Standard (DES) algorithm.

At the algorithmic level, in a first part, an investigation is made of algorithmic transformations which conserve the behavior of the DES algorithm. Out of these transformations, a selection is made which leads to a very modular and pipelined data path architecture for the **cryptographic** co-processor.

In a second part, algebraic algorithms, which occur in many real-time multi-dimensional signal processing applications, are investigated for an ASIC implementation. Examples which have been investigated are: a one-chip VLSI implementation for the separation of biomedical signals, QR decomposition, the Durbin algorithm to solve a Toeplitz system, etc.

At the architecture level, in a first part, a new **controller** architecture and design methodology is developed for applications which require both a high throughput and a high degree of programmability within the application domain. The proposed **controller** architecture consists of a hierarchy of pipelined, communicating **finite state machines** . Applied to the design of the **cryptographic** processor, it resulted in the fastest and most programmable **cryptographic** processor, known in literature.

In a second part, a high level memory management strategy is proposed. Indeed, real-time algebraic applications are heavily based on matrix and vector operations and the memory organization defines often the efficiency of the final realization.

At the silicon assembly level, a new approach for automatic electrical verification is described. For a library of basic cells, a set of construction rules are defined which guarantee a correct electrical behaviour of the composed circuit. The same construction rules are coded in an expert system, which verifies again the extracted layout.

31/5/4 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5131870 INSPEC Abstract Number: C9604-6130S-003
Title: Linear models for keystream generators
Author(s): Golic, J.D.
Author Affiliation: Inf. Security Res. Centre, Queensland Univ. of Technol., Brisbane, Qld., Australia
Journal: IEEE Transactions on Computers vol.45, no.1 p.41-9
Publisher: IEEE,
Publication Date: Jan. 1996 Country of Publication: USA

CODEN: ITCOB4 ISSN: 0018-9340
[illegible]: 0018-9340(199601)45:1L.41:LMKG;1-N
[illegible] Identity Number: I071-96002
[illegible] Copyright Clearance Center Code: 0018-9340/96/$05.00
Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: It is shown that an arbitrary binary keystream generator with M bits of memory can be linearly modeled as a non-autonomous linear feedback shift register of length at most M with an additive input sequence of nonbalanced identically distributed binary random variables. The sum of the squares of input correlation coefficients over all the linear models of any given length proves to be dependent on a keystream generator. The minimum and maximum values of the correlation sum along with the necessary and sufficient conditions for them to be achieved are established. An effective method for the linear model determination based on the linear sequential circuit approximation of autonomous **finite - state machines** is developed. Linear models for clock controlled shift registers and arbitrary shift register based keystream generators are derived. Several examples including the basic summation generator, the clock-controlled cascade, and the shrinking generator are presented. Linear models are the basis for a general structure-dependent and initial-state-independent statistical test. They may also be used for divide and conquer correlation attacks on the initial state. **Security** against the corresponding statistical attack appears hard to control in practice and generally hard to achieve with simple keystream generator schemes. (25 Refs)
Subfile: C
Descriptors: **cryptography** ; **finite state machines** ; shift registers
Identifiers: keystream generators; linear feedback shift register; binary [illegible] Machines; **finite - state machines** ; shift register; divide and [illegible] correlation attacks; clock-controlled shift registers; correlation [illegible]; **cryptography** ; linear models
Class Codes: C6130S (Data security); C4230D (Sequential switching theory) ; C4220 (Automata theory)

31/5/5 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5120100 INSPEC Abstract Number: B9601-6120B-033, C9601-6130S-026
Title: Linear cryptanalysis **of stream** ciphers
Author(s): Golic, J.D.
Author Affiliation: Inf. Security Res. Centre, Queensland Univ. of Technol., Brisbane, Qld., Australia
Conference Title: Fast Software Encryption. Second International Workshop. Proceedings p.154-69
Editor(s): Preneel, B.
Publisher: Springer-Verlag, Berlin, Germany
Publication Date: 1995 Country of Publication: West Germany vii+366 pp.
ISBN: 3 540 60590 8
Conference Title: Fast Software Encryption. Second International Workshop. Proceedings
Conference Sponsor: Europay Int.; Microsoft; Uti-maco Belgium
Conference Date: 14-16 Dec. 1994 Conference Location: Leuven, Belgium
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Starting from recent results on a linear statistical weakness of keystream generators and on linear correlation properties of combiners with memory, linear **cryptanalysis** of stream **ciphers** based on the linear sequential circuit approximation of **finite state machines** is introduced as a general method for assessing the strength of stream **ciphers** . The statistical weakness can be used to reduce the uncertainty of unknown plaintext and also to reconstruct the unknown structure of a keystream generator, regardless of the initial state. The linear correlations in arbitrary keystream generators can be used for divide and conquer correlation attacks on the initial state based on known plaintext

or **ciphertext** only. Linear **cryptanalysis** of irregularly clocked shift registers as well as of arbitrary shift register based binary keystream generators proves to be feasible. In particular, the direct stream **cipher** mode of block **ciphers** , the basic summation generator, the shrinking generator, the clock controlled cascade generator, and the modified linear congruential generators are analyzed. It generally appears that simple shift register based keystream generators are potentially vulnerable to linear **cryptanalysis** . A proposal of a novel, simple and **secure** keystream generator is also presented. (31 Refs)

Subfile: B C

Descriptors: **cryptography** ; divide and conquer methods; **finite state machines** ; sequential circuits; shift registers

Identifiers: linear **cryptanalysis** ; stream **ciphers** ; linear statistical weakness; keystream generators; linear correlation properties; linear sequential circuit approximation; **finite state machines** ; statistical weakness; unknown plaintext; divide and conquer correlation attacks; arbitrary keystream generators; **ciphertext** ; irregularly clocked shift registers; binary keystream generators; direct stream **cipher** mode; block **ciphers** ; basic summation generator; shrinking generator; clock controlled cascade generator; modified linear congruential generators

Class Codes: B6120B (Codes); C6130S (Data security); C4220 (Automata theory); C4230D (Sequential switching theory)

31/5/6 **(Item 3 from file: 2)**

5039172 INSPEC Abstract Number: B9510-6120B-037, C9510-6130S-017

Title: Intrinsic statistical weakness of keystream generators

Author(s): Golic, J.D.

Author Affiliation: Inf. Security Res. Centre, Queensland Univ. of Technol., Brisbane, Qld., Australia

Conference Title: Advances in Cryptology - ASIACRYPT'94. 4th International Conference on the Theory and Applications of Cryptology. Proceedings p.91-103

Editor(s): Pieprzyk, J.; Safavi-Naini, R.

Publisher: Springer-Verlag, Berlin, Germany

Publication Date: 1995 Country of Publication: West Germany xii+430 pp.

ISBN: 3 540 59339 X

Conference Title: Advances in Cryptology - ASIACRYPT '94. 4th International Conference on the Theory and Applications of Cryptology

Conference Sponsor: Univ. Wollongong

Conference Date: 28 Nov.-1 Dec. 1994 Conference Location: Wollongong, NSW, Australia

Language: English Document Type: Conference Paper (PA)

Treatment: Theoretical (T)

Abstract: It is shown that an arbitrary binary keystream generator with M bits of memory can be linearly modelled as a non-autonomous linear feedback shift register of length at most M with an additive input sequence of unbalanced identically distributed binary random variables. An effective method for the linear model determination based on the linear sequential circuit approximation of autonomous **finite - state machines** is developed. Linear models for clock-controlled shift registers and arbitrary shift register based keystream generators are derived. Several examples, including the time-variant memoryless combiner, the basic summation generator, the stop-and-go cascade, and the shrinking generator are presented. Linear models are the basis for a general structure-dependent and initial-state-independent statistical test, and they may also be used for correlation attacks on the initial-state. Theoretical **security** against the introduced statistical attack appears hard to control in practice and hard to achieve with simple schemes. (21 Refs)

Subfile: B C

Descriptors: binary sequences; correlation methods; **cryptography** ; **finite state machines** ; random processes; sequential circuits; shift registers; statistical analysis

Identifiers: intrinsic statistical weakness; arbitrary binary keystream generator; non-autonomous linear feedback shift register; additive input sequence; nonbalanced identically distributed binary random variables; [illegible] sequential circuit approximation; autonomous **finite - state machines** ; clock-controlled shift registers; time-variant memoryless [illegible] basic summation generator; stop-and-go cascade; shrinking [illegible] initial-state-independent; statistical test; correlation attacks ; [illegible] **security** ; introduced statistical attack
Class Codes: B6120B (Codes); B0240Z (Other topics in statistics); C6130S (Data security); C1140Z (Other topics in statistics); C4220 (Automata theory)

31/5/7 **(Item 4 from file: 2)**
DIALOG(R)File 2:INSPEC

[illegible]9609 INSPEC Abstract Number: B9406-0100-101, C9406-0310D-012
Title: Proceedings of NetSec '93. Network Security in the Open Environment
Publisher: Comput. Security Inst, San Francisco, CA, USA
Publication Date: 1993 Country of Publication: USA 921 pp.
Conference Title: Proceedings of NetSec '93. Network Security in the Open Environment
Conference Date: 21-23 June 1993 Conference Location: Washington, DC, USA
Language: English Document Type: Conference Proceedings (CP)
Abstract: The following topics were dealt with: LANs; **encryption** ; [illegible]lnerability assessment for telecommunications network recovery; network [illegible] and procedures; contingency planning; **security** awareness [illegible] microcomputer networks; employees; disasters; information **security** ; information protection; a European perspective; **security** [illegible]; the downside of computer and communications **security** ; privacy; **security** policies; the open systems challenge; **safe** communications outside the company; UNIX; EDI; intrusion detection and enterprise-wide networks; virus protection; TCP/IP; PBX fraud; hackers and crackers; Kerberos **authentication** services; Internet mail; facsimile; leading-edge technology; **security** models; SNMP protocol; electronic document authorization; risk analysis; auditing; countermeasures to network attacks; **security** administration and management; the two- **state machine** ; client/server systems; Novell NetWare; **securing** VTAM; guarding the mainframe; CA-ACF2; DECNET; CA-Top Secret; IBM token ring networks; Tandem systems; Ethernet; OS/2; and academic environments.
Subfile: B C
Descriptors: computer networks; DP management; open systems; **security** of data
Identifiers: network **security** ; open environment; LANs; **encryption** ; disasters; **security** policies; open systems; protocol; **security** administration; Novell NetWare
Class Codes: B0100 (General electrical engineering topics); B0140 (Administration and management); B6210L (Computer communications); C0310D (Installation management); C5620 (Computer networks and techniques)

31/5/8 **(Item 5 from file: 2)**
DIALOG(R)File 2:INSPEC

[illegible] INSPEC Abstract Number: B84053420, C84044876
Title: Formal verification of a secure network with end-to-end [illegible]cryption
Author(s): Britton, D.E.
Author Affiliation: RCA Government Systems Div., Camden, NJ, USA
Conference Title: Proceedings of the 1984 Symposium on Security and Privacy p.154-66
Publisher: IEEE Comput. Soc. Press, Silver Spring, MD, USA
Publication Date: 1984 Country of Publication: USA vi+227 pp.

ISBN: 0186 0532 4
U.S. Copyright Clearance Center Code: CH2013-1/84/0000-0154$01.00
Conference Sponsor: IEEE
Conference Date: 29 April-2 May 1984 Conference Location: Oakland, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: A formal specification and verification of a simple **secure** communications network using end-to-end **encryption** is presented. It is shown that for a network of this type all data sent over the network is **encrypted** and all hosts on the network exchange messages only if they are authorized to do so. The network and its hosts are modeled by a set of concurrent processes that communicate via unidirectional buffers. Each process is viewed as a **state machine** . The specification has been formally verified using the commercially available VERUS verification system. (10 Refs)
Subfile: B C
Descriptors: communication networks; **cryptography** ; encoding
Identifiers: **secure** network; end-to-end **encryption** ; formal specification; verification; communications network; network exchange messages; concurrent processes; unidirectional buffers; VERUS verification system
Class Codes: B6120B (Codes); B6210 (Telecommunication applications); C6150 (Data communication equipment and techniques); C6130 (Data handling techniques)

31/5/9 **(Item 1 from file: 6)**
DIALOG(R)File 6:NTIS
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1469687 NTIS Accession Number: AD-A212 351/1
Matrix Model for the Linear Feedback Shift Register
(Final rept. Jun-Aug 87)
Wardlaw, W. P.
Naval Research Lab., Washington, DC.
Corp. Source Codes: 000927000; 251950
Report No.: NRL-9179
6 Jul 89 19p
Languages: English
Journal Announcement: GRAI9002
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NTIS Prices: PC A03/MF A01
Country of Publication: United States
Contract No.: W1253
In this report, a matrix model is used to discover some of the properties of the linear feedback shift register (LFSR) and to consider its application to **security** systems. First the hardware and operation of the LFSR is briefly discussed. Then a representation of the LFSR as a **finite state** device is used to obtain the matrix model for the LFSR. The matrix model is employed to derive a number of known results about the period of the LFSR as well as some new results concerning subperiods of an LFSR. **Cryptographic** applications are suggested by the randomness properties of the LFSR bit stream output. The matrix model provides a concise treatment of the **cryptanalysis** of the simple LFSR system. Some suggestions are made to improve the **security** of LFSR secrecy systems. (RRH)
Descriptors: **Cryptography** ; *Feedback; *Linear systems; *Shift registers ; Output; **Security** ; Streams
Identifiers: NTISDODXA
Section Headings: 62GE (Computers, Control, and Information Theory--General); 62C (Computers, Control, and Information Theory--Control Systems and Control Theory)

31/5/10 **(Item 2 from file: 6)**

DIALOG(R)File 6:NTIS

1020159 NTIS Accession Number: AD-A124 820/2
Secure **Computer Network**
(Master's thesis)
Steinmetz, J. S.
Air Force Inst. of Tech., Wright-Patterson AFB, OH. School of Engineering.
Corp. Source Codes: 000805002; 012225
Report No.: AFIT/GCS/EE/82D-34
Nov 82 114p
Languages: English Document Type: Thesis
Journal Announcement: GRAI8313
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A06/MF A01
Country of Publication: United States
In this thesis, the initial design for a **secure** computer network is developed. The requirement for a **secure** computer network is based on the need to protect sensitive and personal information currently processed by computer networks. The concepts of physical **security** , reference monitors, **encryption** , and network protocols are presented. Then, the top-level design of the **secure** computer network is developed. This design consists of **secure** data bases controlled by Kernelized **secure** operating systems which are connected by a **secure** communications subnetwork. The phases of **secure** communications: location, identification, request, and request response are discussed. A model for the **secure** communications subnetwork is then presented. This model relies on two major components: **Secure** Network Interface Computers (SNICs) and a Network Directory and **Security** Server (NDSC). A **finite state** analysis of the communication channels demonstrates the **security** of the model. Recommendations are presented to facilitate the development of this **secure** network. (Author)
Descriptors: Computers; * **Secure** communications; *Communications networks; Information processing; **Security** ; Experimental design; Requirements; Intrusion detection; Data bases; Operation; Facilities; Theses
Identifiers: Computer networks; Physical **security** ; Kernels operating systems; NTISDODXA
Section Headings: 62B (Computers, Control, and Information Theory--Computer Software); 45C (Communication--Common Carrier and Satellite)

31/5/11 **(Item 1 from file: 144)**
DIALOG(R)File 144:Pascal

12811397 PASCAL No.: 97-0027163
Surete de fonctionnement et securite **informatique**
ARLAT Jean, coord; DUPUY Michel, coord
LAAS-CNRS, Toulouse, France; France-Telecom, Paris, France
Journal: TSI. Technique et science informatiques, 1996, 15 (4) 135 p.
ISSN: 0752-4072 CODEN: TTSIDJ Availability: INIST-19593; 354000066556260000
No. of Refs.: dissem.
Document Type: P (Serial) ; M (Monographic)
Country of Publication: France
Language: French Summary Language: English

English Descriptors: Abstract machine; **Finite state machine** ; Fault tolerant system; **Safety** ; Fragmentation; **Cryptography** ; Identification

French Descriptors: Machine abstraite; Machine etat fini; Systeme tolerant les pannes; **Securite** ; Fragmentation; **Cryptographie** ; Identification

31/5/12 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

04687759 Genuine Article#: BF02R Number of References: 31
Title: THE RAMPART TOOLKIT FOR BUILDING HIGH-INTEGRITY SERVICES
Author(s): REITER MK
Corporate Source: AT&T BELL LABS,CRAWFORDS CORNER RD/HOLMDEL//NJ/07733
Journal: LECTURE NOTES IN COMPUTER SCIENCE, 1995, V938, P99-110
ISSN: 0302-9743
Language: ENGLISH Document Type: ARTICLE
Geographic Location: USA
Subfile: ISTP; SciSearch
Journal Subject Category: COMPUTER SCIENCE, THEORY & METHODS
Abstract: Rampart is a toolkit of protocols to facilitate the development of high-integrity services, i.e., distributed services that retain their availability and correctness despite the malicious penetration of some component servers by an attacker. At the core of Rampart are new protocols that solve several basic problems in distributed computing, including asynchronous group membership, reliable multicast (Byzantine agreement), and atomic multicast. Using these protocols, Rampart supports the development of high-integrity services via. the technique of **state machine** replication, and also extends this technique with a new approach to server output voting. In this paper we give a brief overview of Rampart, focusing primarily on its protocol architecture. We also sketch its performance in our prototype implementation and ongoing work.
Identifiers--KeyWords Plus: DISTRIBUTED SYSTEMS; SIGNATURES
Research Fronts: 94-1454 004 (DISTRIBUTED REAL-TIME SYSTEMS; EFFICIENT ALGORITHM; **SAFETY** -CRITICAL SOFTWARE; MULTIPLE MUTUAL EXCLUSION)
94-4771 001 (OPEN DISTRIBUTED SYSTEMS; SIGNATURE SCHEME; NETWORK **SECURITY** ; **AUTHENTICATION** SERVICE; THRESHOLD **CRYPTOSYSTEM** ; DISCRETE EXPONENTIATION)
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MELLIARSMITH PM, 1990, V1, P17, IEEE T PARALLEL DIST
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REITER MK, 1994, V16, P986, ACM T PROGR LANG SYS
REITER MK, 1994, P68, P 2 ACM C COMP COMM
REITER MK, 1994, P176, 1994 P IEEE S RES SE
RIVEST RL, 1978, V21, P120, COMMUN ACM
SCHNEIDER FB, 1990, V22, P299, COMPUT SURV
SHRIVASTAVA SK, 1992, V41, P542, IEEE T COMPUT
STEINER JG, 1988, P191, P USENIX SWINT C
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VANRENESSE R, 1992, P USENIX MICR OTH KE
VOYDOCK VL, 1983, V15, P135, COMPUT SURV

31/5/13 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

00502306 Genuine Article#: LF707 Number of References: 18
Title: **VERIFICATION AND MODELING OF** AUTHENTICATION **PROTOCOLS**
Author(s): HAUSER RC; LEE ES
Corporate Source: UNIV ZURICH,INST INFORMAT,WINTERTHURERSTR 190/CH-8057 ZURICH//SWITZERLAND/; UNIV TORONTO,DEPT COMP SCI/TORONTO M5S 1A4/ONTARIO/CANADA/
Journal: LECTURE NOTES IN COMPUTER SCIENCE, 1992, V648, P141-154
ISSN: 0302-9743
Language: ENGLISH Document Type: ARTICLE
Geographic Location: SWITZERLAND; CANADA
Subfile: SciSearch
Journal Subject Category: COMPUTER APPLICATIONS & CYBERNETICS
Abstract: With the emergence of numerous distributed services, the importance of electronic **authentication** in networks is rapidly increasing. Many **authentication** protocols have been proposed and discussed. Burrows, Abadi and Needham [BAN1] created alogic of **authentication** to formally analyze **authentication** protocols. This BAN-logic has been subject to critique and several extensions have been suggested. Nonetheless, due to its straightforward design and its ease-of-use, it attracts the attention of current research. In this paper, an **authentication** logic is proposed which is built closely after the BAN-logic. It addressers answers to important criticisms of BAN like the non-disclosure problem, and avoids some newly discovered weaknesses of BAN, e.g. with respect to freshness. It also does not require any idealization which is a major hurdle to the correct usage of BAN. This extended BAN-logic is instrumented as a verification tool which also allows for modelling the different protocol participants as **finite state machines** . Also, actions of intruders, consequences of such intrusions, and the respective counter-measures can be modelled and simulated.
Identifiers--KeyWords Plus: **ENCRYPTION**
Research Fronts: 91-1456 002 (DISTRIBUTED SYSTEMS; REPLICATED DATA; BYZANTINE AGREEMENT; RELIABLE MULTICAST COMMUNICATION; PROTOCOL DESIGN)
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RIVEST RL, 1978, V21, P120, COMMUN ACM
SNEKKENES E, 1991, P171, 1991 P IEEE CS S RES
SOPER RE, 1989, CSRI236 TECH REP
STTEINER JG, 1988, FEB P USENIX WINT C

31/5/14 (Item 1 from file: 266)
DIALOG(R)File 266:FEDRIP

00187031
IDENTIFYING NO.: 0312676 AGENCY CODE: NSF

ITR: Synthesis System for Discrete Event Systems through Solving Equations over Mathematical Machines

[illegible] INVESTIGATOR: Brayton, Robert K

[illegible] ORG.: University of California-Berkeley, Electronics Research [illegible]y, Berkeley, CA 94720

PROJECT MONITOR: Basu, Sankar

SPONSORING ORG.: National Science Foundation, CCR, 4201 Wilson Boulevard , Arlington, Virginia 22230

DATES: 20030801 TO 20040731 FY : 2003 FUNDS: $200,000 (200000)

SUMMARY: An automaton has states and transitions between states; some states are marked as "accepting". Starting from the initial state, a sequence of input symbols causes the automaton to change states in response. If a sequence can cause the automaton to end up at an accepting state, the sequence of input symbols is said to be accepted and is defined to be in the language of the automaton. **Finite state machines** (FSMs) differ from automata in that all states are accepting and each input symbol is divided into an input part and an output part. Automata and FSMs are used to define "regular" languages. Many interesting problems can be defined in terms of automata, FSMs, or Petri nets and the languages involved. These include problems in binary and multi-valued logic synthesis, engineering change, design of discrete **controllers** , logic verification, testing, deriving winning strategies for discrete games, construction of protocols, and **cryptography** . It was observed by our group that these diverse applications could be formalized in a unified way in terms of language solving. In general, these problems can be stated in terms of the synthesis of a subsystem or component, given a known environment and an external specification. The component to be synthesized may already exist, in which case the goal is to provide a better or optimum [illegible]. In other cases, no implementation may yet exist, and the goal [illegible] if such a desired subsystem exists, and if so to find an [illegible] implementation. An example of the former is a digital system as [illegible] on a microchip composed of interacting components. The system may operate correctly as is, i.e. the system already satisfies its external specification, but one of the components should be improved, in terms of speed, cost, power, etc. An example in which an implementation may be unknown is a control system where we are given a "plant" and an external specification, stating that the output of the plant always stays within certain bounds (is stable), and we want to synthesize a Moore type FSM feedback control unit which does the job. "Engineering change", occurs when a system has been almost completely designed, but at the last moment, a bug in its concept requires the system's specification to be changed. A question arises if just one component can be changed while the other components are left alone. In a biological system, the ability to make measurements inside a component is often limited, but a model of the component is required to be synthesized. There can be several ways that two subsystems interact (can be composed). In hardware, typically two components are wired together and their interaction synchronized using a clock; on each clock tick, information is exchanged. In software, the communication is "asynchronous"; information is sent to another component only after enough time has passed so that the other component has had enough "cycles" to compute its result. Such problems can be reduced to solving an equation of the form, ,where X is the unknown component to be derived, A describes the behavior (or environment) of the known part of the system, S is the external specification or desired behavior, is a type of [illegible] composition operator describing how A and X, are to communicate, [illegible] conformance relation stating when the overall system satisfies the [illegible]. Like many systems of equations, the solution may not be [illegible]; hence there is also the problem of finding a "best" solution. Sets [illegible] restricted solutions that have appropriate additional properties are of interest, e.g. no deadlocks or livelocks, or a solution that is a Moore-type FSM. We propose to: 1. Develop the mathematical tools required for solving equations over various mathematical machines, composition operators and conformance relations. 2. Determine and characterize, for various problem areas, subsets of restricted solutions, which are of practical interest. 3. Develop efficient comp

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